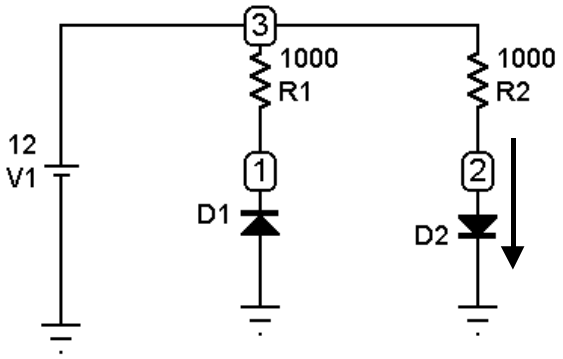
This paper is for engineers that want to use transistors in high speed applications and do not need or want to know how transistors work. The goal is to avoid silicon theory and never talk about electron flow through PN junctions. Hopefully we will discus how to get the most out of a transistor.

Here is some very basic transistor theory. Don't skip over this section, we will be using it soon!

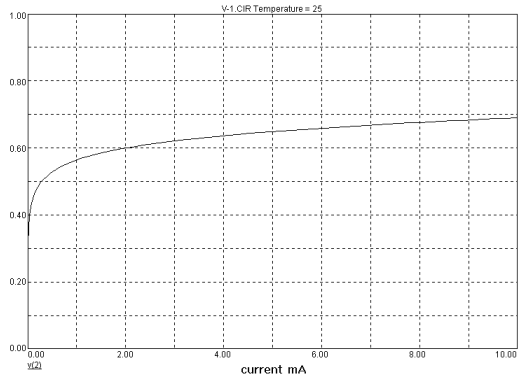
Current will not flow through D1 and will flow through D2. The voltage at point (1) is 12volts, the same as the source. The voltage at point (2) is about 0.7 volts, or what I call one diode drop (1D). It takes about 0.6 to 0.7 volts for a silicon diode to conduct. If the battery V1 is 0.3 volts then there would be no current flow in either diode.



Silicon diode 0.7 volts
Schottky diode 0.34 volts
Germanium diode 0.30 volts

With this diode it takes 0.4 volts to get any current to flow. At 0.56 volts and 1mA the curve flattens out. In the 2 to 10mA range (a 5:1 change) the voltage only changes 15%. This slope extends out to 40mA and only increases slightly at 100mA.
At high currents the impedance is very low. At low voltage the impedance climes fast.

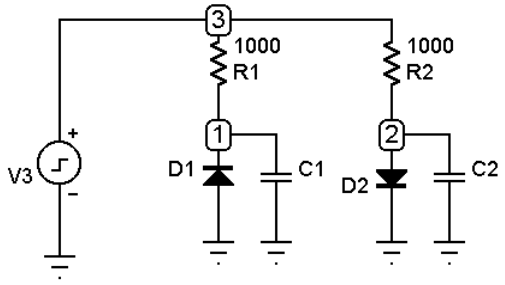
V Volts	I MA	R Ohms
0.90	80.	11
0.80	40.	20
0.70	12.	58
0.65	5.5	118
0.60	2.0	300
0.55	0.9	611
0.50	0.3	1,666
0.45	0.1	4,500
0.40	0.03	13,333



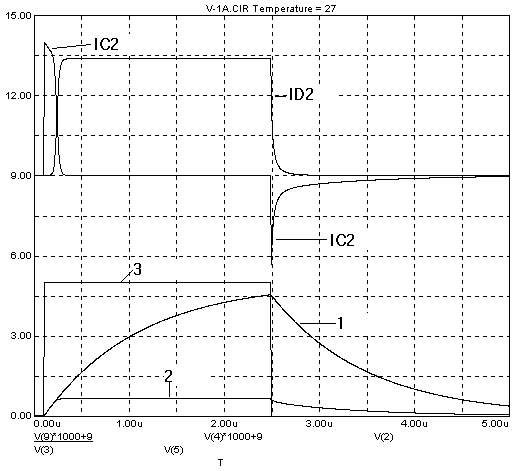
X is 0 to 10mA Y is 0 to 1 volt
Diode is 1N914

All semiconductors have capacitance. To model this capacitance we are placing a capacitor across the part. Now the effects of semiconductor capacitance can be studied.

Pull out the Capacitor and place it externally across the part.



Trace 3 is from the signal source V3. (0 to 5 volts)
Trace 1 is the top if D1. (typical RC delay)
Trace 2 is the top if D2. It starts out with a typical RC delay but soon runs into the diode forward voltage limit. Trace IC2 shows that the entire current is flowing into C2 until the voltage reaches about 0.5 volts. The current switches from IC2 to ID2 in the 0.5 through 0.7 voltage range.

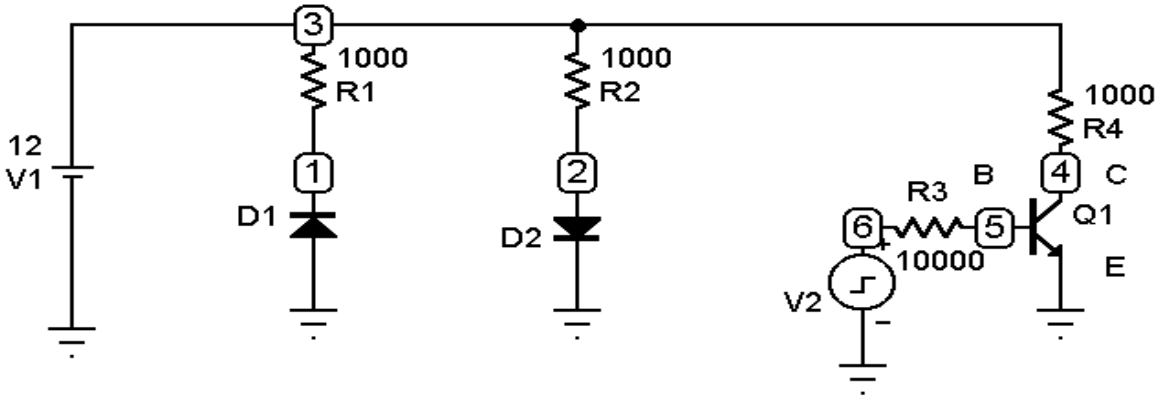


In the 0 to 0.5 voltage region the delay is totally a function of R2 C2. By 0.6 volts the impedance of D2 has dropped to around 600 ohms which is in parallel with R2. (600||1000=375) @ 0.6V At 0.7 volts we have 58||1000=55 ohms. It is clear the RC time is much faster.

⇒It is important to know the impedance of a point when determining the RC time delay.

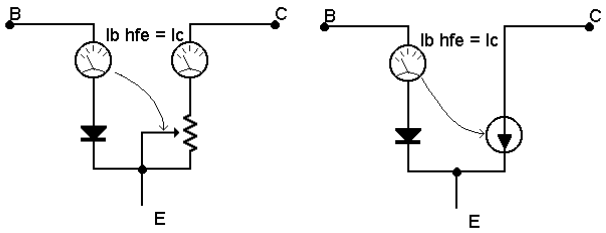
Why does IC2 start out at a peak of 5mA, while the highest point of ID2 is only 4.3mA?

Transistor Q1 looks much like two diodes. There is a diode from base (B) to emitter (E) that acts much like D2. If voltage source V2 is more that 1D (0.6 volts) then there is base current. If V2 is less than 1D then there is no base current. Another diode is from base to collector (C) it does not pass current, much like D1 {if there is no base current}.



Transistors are current amplifiers. If Q1 has a current amplification of 50, then one unite of current in the base will cause the transistor to <u>try</u> to pull 50 unites of current through the collector.

This transistor model uses a base emitter diode, and two current meters. The base current is observed and used to adjust the CE rheostat in an attempt to maintain the output current h_{FE} times larger.



A more accurate model uses a CE current source. If possible the collector current is h_{FE} times the base current.

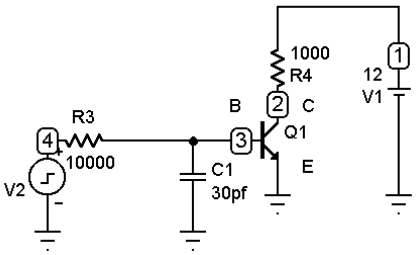
h_{FE} and ß is the ratio of collector current to DC base current

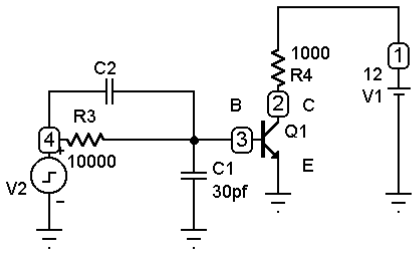
Grounded emitter saturated switch

What can make this amplifier slow? There are many things that slow down this type of grounded emitter amplifier.

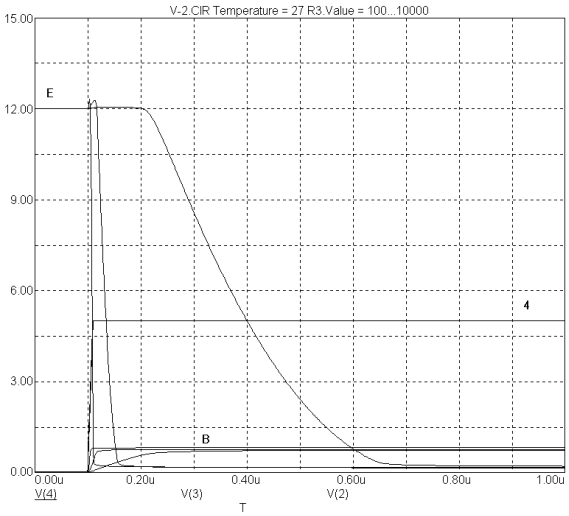
1.) Input impedance-base capacitance delay.

Transistors inherently have base-emitter capacitance, which combined with the input impedance of the amplifier form a RC low pass filter. For the calculations to work right the output impedance of the preceding stage must be added to R3. In this case if V2 had an impedance of 2000 ohms it must be added in to the equation. The printed circuit board trace from R3 to Q1-B adds additional capacitance. Capacitor C1 represents the capacitance found on node 3, mostly due to Q1. Capacitor C2 is an input speedup capacitor used to reduce the effects of base capacitance.





This graph shows three conditions, where R3=100, R3=1,000 and R3=10,000 ohms. The input voltage (4) starts at 0 volts. At time 0.10u it rises to 5 volts. The base-emitter voltage (B) starts out at 0 volts. After time 0.10u it moves upward to 0.7 volts following a typical RC delay. The three curves are for 100, 1,000 and 10,000 ohms input resistance. The output voltage (E) starts at 12 volts. When the B-E voltage of Q1 reaches 1D the output drops to 0.2 volts.



⇒Input impedance should be kept small. On the printed circuit board keep the base node short for both high speed and low noise. Add an input speed up capacitor. The output impedance of the preceding stage should be low.

Why does the collector voltage increase above the supply voltage for a short period of time? Hint: Base collector capacitance.

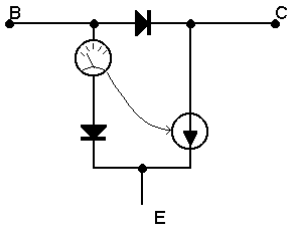
Turn on delay of ≈ 2, 20 and 200nS.

2.) Input impedance base capacitance class A

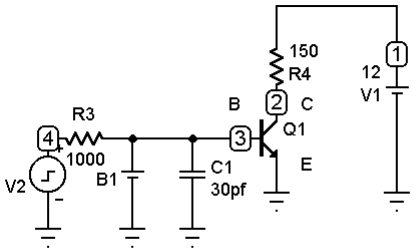
In this example the transistor is asked to switch between two operating points. The base current will move from 1ma to 10ma. From the first graph of Vforward / current this will require the base voltage to move from 0.56 to 0.70 volts, an increase of 0.14 volts. The base impedance will move from 600 down to 60 ohms. Because of the lower impedance the RC time constant will be relatively short but very much a part of the speed equation.

At this point it looks like if the signal source had zero impedance and if R3 is also zero ohms then the transistor would be infinitely fast. There is a hidden impedance inside the base of each transistor. The MPSH20 transistor has a base spreading resistance (r'_b) of 20 ohms.

3.) Storage delay



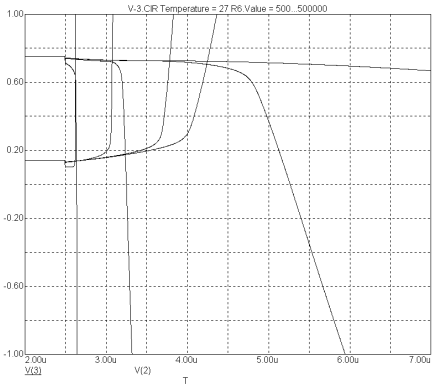
There is a turn off delay that goes beyond the B-E capacitance. When there is base collector current the transistor becomes harder to turn off. To explain Ibc current look at the transistor model to the right. The BC diode has a slightly lower turn on voltage then the BE diode. A typical Vbe is 0.7 volts and a typical Vbc is 0.55 volts. When the Vce drops into the range of 0.15 volts base current passes through both diodes. The current through the BE diode is just enough to pull the collector down to 0.15 volts. Any excess base current passes through the base collector diode. If this paper talked about silicon theory we would need to study minority carriers stored in the base–collector junction. To avoid that, we could talk about a storage device like a battery that exists in the B-C junction.



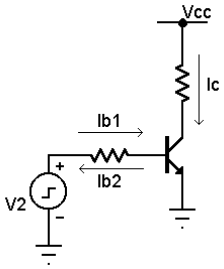
In a saturated condition the collector and emitter are 'stuck' together. Because the C and E are almost at the same voltage, the BC "battery" looks like a BE "battery". To make things easier to explain I will model the storage delay/ base charge effect as a battery from base to emitter that is only present when the transistor is in saturation. In this figure the base capacitance is still there as C1. Across the base is B1 that charges only when there is excess base current; when part of the base current is flowing into the collector.

Large high voltage power transistors have long pronounced storage delay times that are easy to study. A 1000 volt 10 amp 150 watt transistor may take 3micro seconds to turn off the base even when the base is being pulled off with 5 amps. This effect is in all transistors but is harder to see in small transistors. It takes current and time to charge a battery. The time verses charge curve appears to be exponential. In the case of the 1000 volt 10 amp transistor it took 1uS to charge to 50% and 9uS more to charge to 95%. If the base was over driven for more than 10uS little more charge is added to the battery. If Q1 was only slightly over driven then little current is stored in B1. If the base current is many times what is needed to bring the C-E voltage down to under 0.7 volts then B1 will have a large charge. It is important to note that the base charge effect is a turn off effect not a turn on effect.

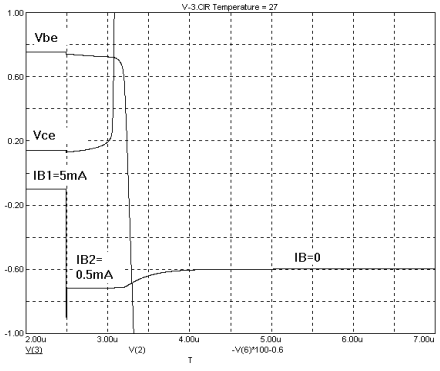
A transistor that is on can be turn off by removing base current. Unfortunately there is charge stored on C1 and B1 that will keep Q1 turned on. Energy stored in B1 will hold the B-E voltage up until the entire charge has been dumped through the base emitter junction. Only then can C1's charge be discharged through the base. This process keeping the transistor on for a long time.



If speed is needed all base charges must be pulled out of Q1. The symbol IB1 is the turn on current sent into the base. If a saturated transistor is to be turned off fast negative current must be pulled out of the base, called IB2.



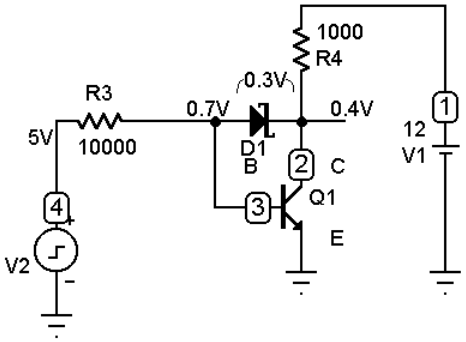
This graph shows C-E and B-E voltage under four different conditions of IB2. IB2= 10mA, 1mA, 100uA and 10uA. The stored energy in the base is pulled out by .127u, .5u, 1u and 1.5u second. After that the downward slope is a function of base capacitance and negative base current. IB1 is 5mA for all curves.



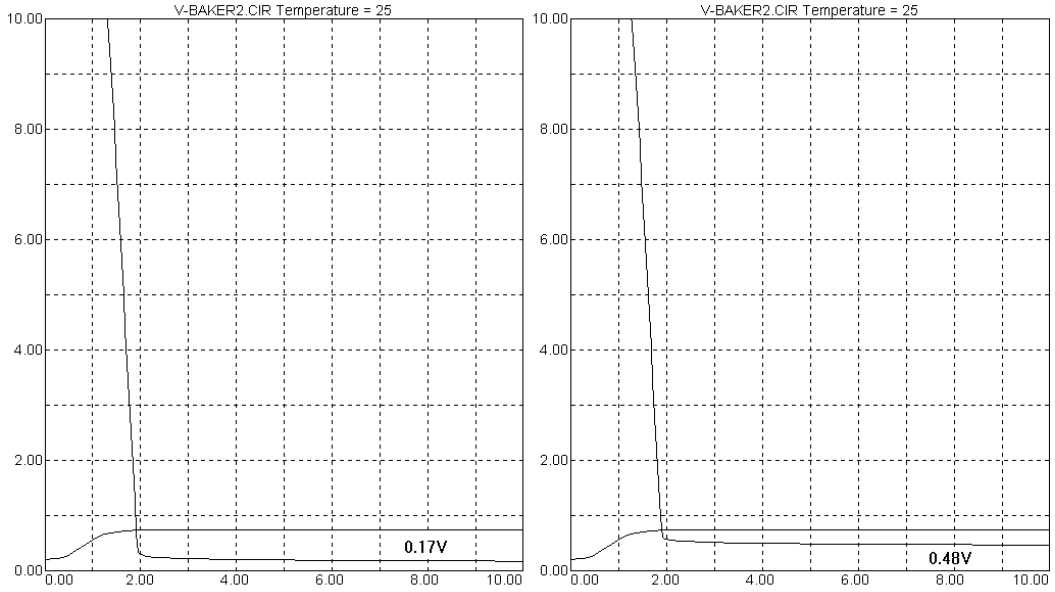
Volts/second=current/capactance

The collector emitter voltage (Vce) starts out at about 0.15 volts and after the transistor opens up, it heads upward off the graph. The Vbe voltage starts out at 0.78 volts with an IB1 current of 5mA. At time 2.5uS a negative base current called IB2 discharges the base storage "battery" at a rate of 0.5mA. After the battery is discharged the base is free to be pulled negative.

4.) Baker Clamp

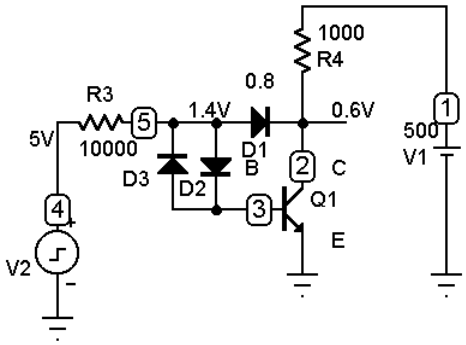


Storage time is a severe limitation to the speed performance of saturated switches. One solution is to not allow the switch to saturate. A Schottky clamping diode is connected from base to collector in a manner as to steel excess base current and hold the transistor just out of saturation. The Schottky diode has a forward drop if less than that of the base-emitter junction of a silicon diode. Base current passes through R3 into the base of Q1. If too much base current is applied to Q1 then the Vce voltage will be low. A low collector voltage will cause D1 to conduct steeling away excess base current. The Vforward of the Schottky diode is 0.3volts while the silicon transistor has a Vforward of 0.7 volts.

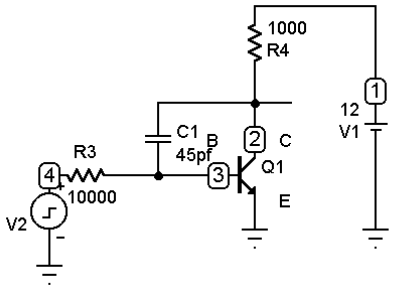


Vce & Vbe with out clamping and Vce & Vbe with clamping.
X=0 to 10 volts of V2 Y=0 to 10V for Vce & Vbe

Until recently high voltage Schottky diodes were not available. When Baker clamping high voltage transistors a high voltage diode must be used. The problem is that high voltage diodes have high forward voltage. In our example the Baker clamping diode has a forward voltage of 0.9 volts. The Vbe of Q1 needs to be greater than the forward voltage of the clamping diode. To increase the effective Vbe of Q1 a diode D2 is added. Diode D3 is added to aide in Q1 turn off. Signal source can remove Q1 base charge via R3 and D3.



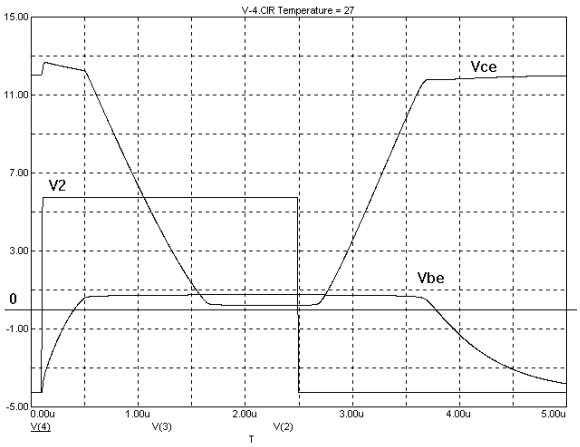
5.) Miller Effect studied as an integrator



The base collector capacitance (Ccb) seriously impacts the performance of high speed amplifiers. The Ccb is a feedback capacitor because it is placed from input to output of the amplifier. If the amplifier has a large voltage gain then the effects of the capacitor will be large. The grounded emitter amplifier we are studying has a large voltage gain.

There are several different ways of studying the Ccb effect. To totally confuse the reader we will study the integrator method here and use a second model later in the paper.

Node 3, the base of Q1 operates at about 0.7 volts. The signal source V2 has a waveform that has been shifted upward by 0.7 volts to compensate. The signal from V2 is +5.7 and –4.3 volts. Capacitor C1 is simulating Ccb. When V2 is at +5.7 volts there will be 5 volts across R3 causing 500uA to flow into the base of Q1. The transistor will start to turn on, pulling it's collector down. As the top of C1 is forced down, the bottom of C1 will push down on Q1-base turning it back off. The results is the 500uA from R3 will be counter by an equal 500uA passed through C1. Actually there will be about 60uA offset caused by the fact it takes that much current to keep Q1 biased on.



⇒Lets do the math.
It 500uA is passing through a 45pF capacitor what is the change in voltage across Ccb?

(500uA / 45pF) = 11volts/micro second

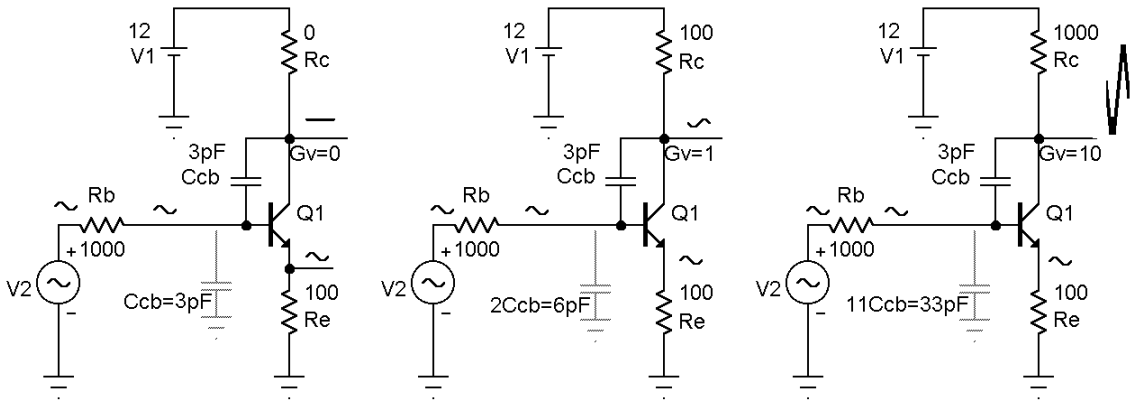
By looking at the graph it can bee seen that the collector moves from 12 volts to 1 volt in 1u second.

When V2 pulls R3 negative Q1 turns off. This causes the collector voltage to increase. Current passes through the collector-base capacitor to keep the base turned on. Resistor R3 is removing 500uA from the base while Cce is putting the same amount of current back into the base.
⇒Once again keep the input impedance low.

Grounded emitter non-saturated

Grounded emitter amplifiers with high gain will have serious Ccb problems. An amplifier with voltage gain will respond to a small input signal with a larger inverse signal. The input signal is on the lower end of Ccb. The upper end of Ccb will have a signal Gv times larger and inverted. The A.C. signal across Ccb is Gv+1. The effective size of Ccb is multiplied by 1 + the voltage gain of the amplifier. An amplifier with a gain of 10 will have an effective Ccb of 11Ccb.

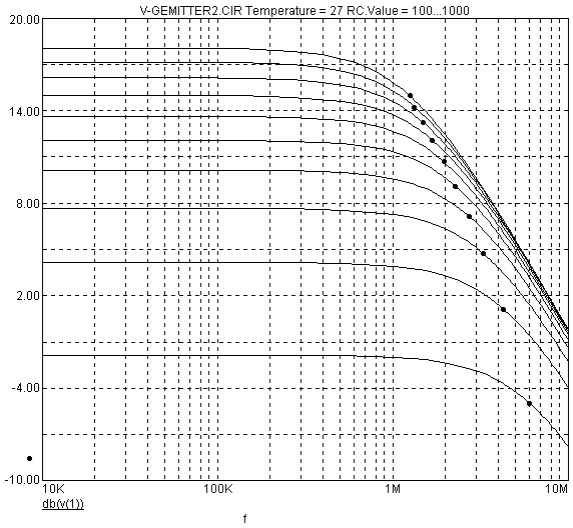
Ccb effective = (1+Gv)Ccb



In proof, the first amplifier has a gain of 0. The Ccb of 3pF has the input voltage across Ccb. The second amplifier has twice the input signal across Ccb. In the last amplifier eleven times the input signal appears across Ccb.

A graph shows gain and frequency response when Rc is varies from 100 to 1,000 in steps of 100 ohms. The gain is from 1 to 10. The effective value of Ccb if from 6 to 33pF. The –3bd point is from 6mhz to 1.1mhz.

⇒Keep Ccb small! Keep Gv small! If large gain is needed, use a different type of amplifier or use more than one amplifier.

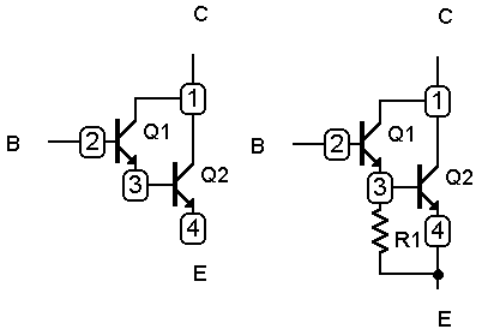


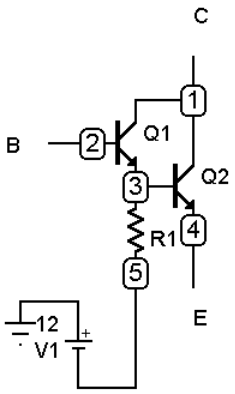
Base Spreading resistance

High frequency transistors often specify a collector-base time constant. (R'_b Ccb) The MPSH20 transistor quotes a R'_b Ccb = 10ps. The Ccb is 0.5pF. This implies a base resistance of 20 ohms. Usually an extra 5 to 20Ω of base resistance will not effect you circuit.

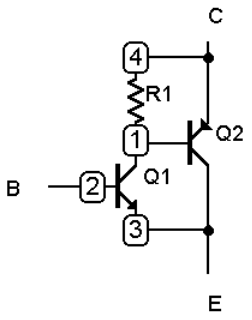
Darlington

Two transistors connected together act like a single transistor with large current gain. This is very handy where high currents are involved or for high input impedance. The Vbe is twice normal. The Vsat or the minimum Vce is 0.7 volts more than normal. Transistor Q1 can be driven to saturation but Q2 can not. Leakage current through Q1ce will pass into Q2 and be amplifier by the current gain of Q2. Over temperature extremes the Darlington will have large leakage current unless a resistor is added from Q2be. The value of this resistor needs to pass the worst case Q1's leakage current with out developing 0.5 volts.





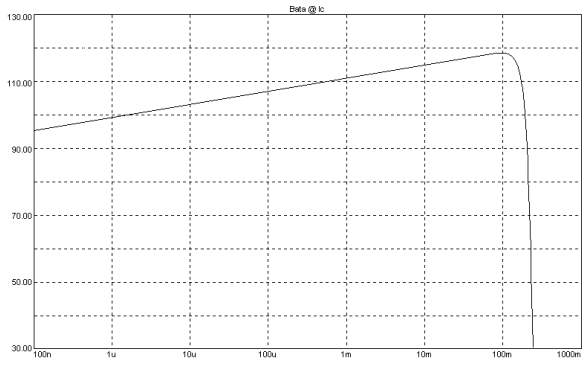
For high speed applications Q1 can turn Q2 on but Q1 can not turn Q2 off. This leaves the Darlington very slow. Add a base emitter resistor on Q2 for turn off purposes. For very high speed application more than 0.7 volts should be placed across R1. In this example R1 discharges Q1's base by a negative 12 volt supply. The added base resistor reduces the Darlington's current gain.



There is a similar high Beta version called a complementary Darlington or a Sziklai Darlington. The Vbe is only one diode drop. The Vsat is greater than 1D. In this example Q1 is NPN so the Darlington acts NPN. R1 is used for both leakage current and Q2 turn off.

Beta limit

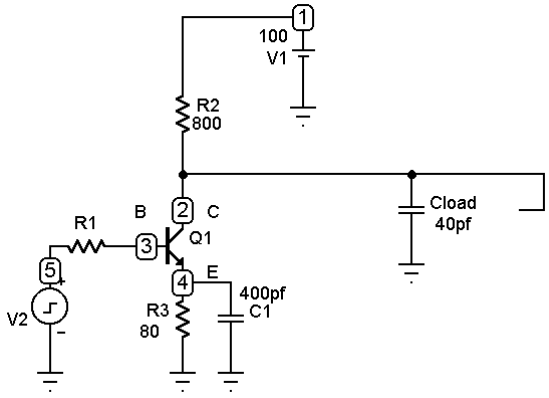
The current gain is dependent on the collector current (Ic). This graph shows the current gain and collector current for the 2SC4439 transistor. At 0.1uA the gain is 95. The gain rises to a maximum of 127 at 100mA and falls rapidly to 30 at 250mA. It should be noted that the 100mA to 250mA area of the curve is unpredictable.



What is Beta limiting? If the signal source driving this transistor could only output 8mA then this transistor would Beta limit its collector current at 250m amp. (8mA X 30 ß = 240mA)

The 2SC4439 is a video output transistor having low capacitance, high collector voltage (150 volts) and a Ft of 400mhz. By looking at the graph of current gain and Ic it might be determined that this transistor will operate well at 100mA of collector current. Keep in mind that; (for speed) keep the current high and the impedance low.

In our example the signal source driving Q1 is only capable of delivering 8mA. Lets pretend that Q1 does not have any input or output capacitance. The video amplifier is driving a 40pF load that is comprised of a CRT cathode, Tube socket, arc protection components and wiring.



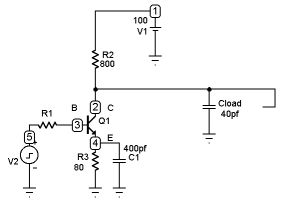
Cload slows the amplifier down. C1 attempts to speed up the amplifier at the same point. For the sake of this example Q1 is biased so Ic is near 100mA. Signal source V2 applies 8mA into the base of Q1. With 8mA of base current Q1 Ic will be limited to 250mA. Resistor R2 supplies 100mA and the remaining 150mA discharges Cload.

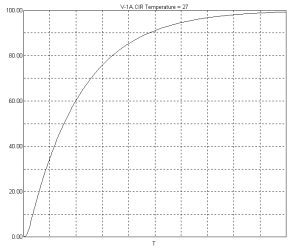
⇒What is the rate of discharge of Cload at 150mA? 150mA/40pF = 3.75 volts/nano-second A 45 volt swing takes 12nS.

In this example current from R2 uses up nearly half of the current capably of Q1. When high speed amplifiers drive capacitance loads the A.C. collector current will be higher than the D.C. model suggests.

Load resistance

In this single transistor output stage amplifier the pull down speed is directly related to transistor Q1. The pull up speed is dependent on R2. The maximum pull up speed is limited by R2 and Cload. They form an RC time constant. It takes current through R2 to move the load capacitance. To get current it takes voltage across the load resistor R2. The rise time rate gets very slow as the output approaches the supply voltage.



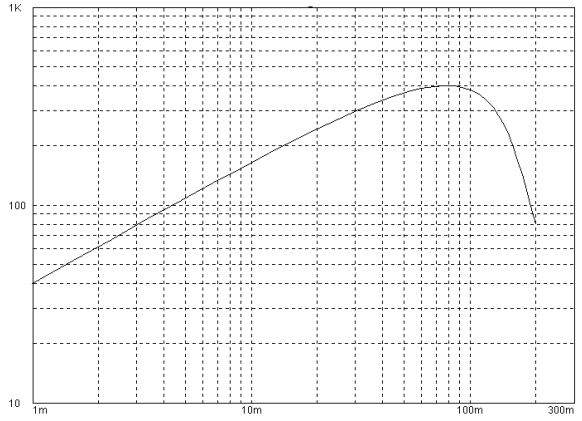


Vout = 20 volts VR2 = 80 volts 100ma 2.5v/nS
Vout = 92 volts VR2 = 8 volts 10ma 0.25v/nS
Vout = 99.2 volts VR2 = 0.8 1ma 0.025v/nS

⇒It takes current to move the output fast. Collector resistance must be low. Keep voltage across the collector resistor.

f_T and collector current

Input capacitance has an effect even with a low impedance signal source. The current through Cbe is not amplified by the transistors current gain. At high frequencies much of the base current is stolen away by Cbe. At a frequency of f_T the transistors small signals gain h_{FE} drops to unity.

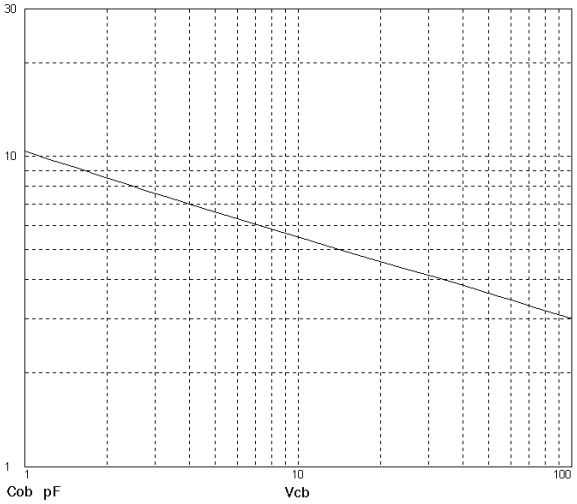


The graph of f_T and Ic for the 2SC4439 shows the transistor is fastest at a Ic of 80mA and a f_T of 400mhz. Low Ic current causes a slow transistor f_T=40mhz at 1mA. Excess collector current also causes a slow transistor f_T=80mhz at 200mA.

⇒Try to keep the transistor operating near the peak of the f_T Ic curve.

Collector Voltage / Transistor Capacitance

The feedback and output capacitances (Ccb, Cce) is a combination of several different factors. The transistor junction capacitance is usually dominate. There is a relatively small transistor lead capacitance and to the PCB trace capacitance. The input source and output load bring along more capacitance.



Transistor junction capacitance behaves like reverse biased diodes, with a value that decreases with increasing back-bias voltage.

$Ccb = k(V-Vd)^n$

V = Vcb
Vd = one diode drop (0.6 volts)
n = -.5 to -.3 depends on process
k = depends on size of dye

Graph of the 2SC4439 video transistor Collector Base Capacitance (Ccb) verses Vcb.

⇒Keep the collector emitter voltage high. For high voltage video power transistors keep Vce above 10 volts. Small 12 volt microwave transistors work fast down to 1 volt Vce.

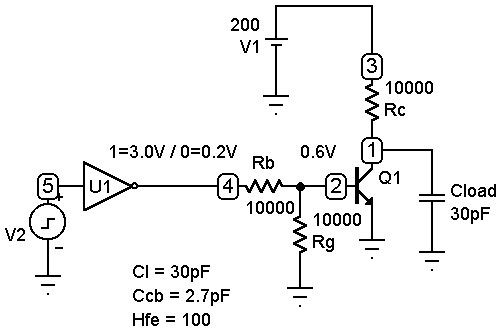
Grounded Emitter High Voltage Driver example rise & fall time
Rise Time

The rise time consists of two factors; the integrator limited rise time and the exponential RC time constant.
Base current: Ib=IRb + IRg IRb = 0.6-0.2V/1000=0.4mA IRg = 0.6v/1000=0.6mA
Ib = 0.4+0.6 = 1.0mA
Slope of rise time using integrator method:
DVc/dt = Ib/Ccb = 1.0mA/2.7pF = 370V/uS
10% to 90% time = 432nS
Collector RC time constant:
RC = 10k * (Ccb + Cl) = 10k * (2.7pf+30pF) = 327nS
The 10% to 90% rise time is 2.2 time constants or 719nS.
If vout = 0 volts then IRc = 200V/10,000 = 20mA. The slope at this point using only the RC model is 20mA/32.7pF or 612V/uS which is faster than the 370V/uS limit of the integrator model. At low output voltages the rise time is slope limited at 370V/uS. The next question is; at what point will the waveform switch to exponential RC limited? The maximum slope of 370V/uS * 32.7pF gives us 12mA of current needed to achieve that slope. To get 12mA through an Rc of 10,000 ohms requires 120 volts across Rc. The results are that at Vout of 80 volts the waveform will switch from slew rate to exponential limited. (200V-120V=80V)

Grounded Emitter High Voltage Driver example rise & fall time
Fall Time

Once again there are two limiting factors, Miller slew rate and Beta limiting.
Ib = IRb + IRg IRb = 3.0v - 0.6V/1000 = 2.4mA IRg = 0.6V/1000 = 0.6mA
Ib = 2.4mA - 0.6mA = 1.8mA
Slope of fall time using integrator method:
dVc/dt = Ib/Ccb = 1.8mA/2.7pF = 667V/uS
10% to 90% time = 240nS

This is an approximation because it did not take into account for base current! To find base current first find collector current. The current through Rc will be in the range of 0 to 20mA depending on Vout. Lets use a value of IRc=10mA. As found earlier collector voltage is moving at a rate of 667v/uS and the load is 30pF+2.7pF this indicates the collector is pulling 22mA from 32.7pF. The TTL inverter is driving 1.8mA into the base of Q1 which is being counter acted by current through Ccb. The collector current is (10+22+1.8)mA. With a hfe of 100 then there muct be an Ib of 0.338mA to get the collector to pass a collector current of 33.8mA. In the D.C. model we found an Ib of 1.8mA. Collector loading suggests an Ib of 0.338mA. 1.8-0.338=1.462 During the output fall time there is an Ib current of 1.45mA that is being offset by Ccb current. If we go back through the formula again dVc/dt = Ib/Ccb = 1.45mA/2.7pF = 537V/uS we get an more accurate answer. The hfe used is at the role off frequency!



This formula is about the same thing and still requires the knowledge of the hfe at the role off frequency.

$$\frac{dVc}{dt} = \frac{1}{Cl + (hfe+1)Ccb} \bullet \left((hfe \bullet Ib) - \frac{VRc}{Rc} \right)$$

The total capacitance is Cload + Ccb times hfe+1. The collector current is Ib times hfe minus the current through Rc. That is 100 X 1.8mA minus 10mA of Rc. Assume a Beta of 100. The output will swing at a rate of 560V/uS.

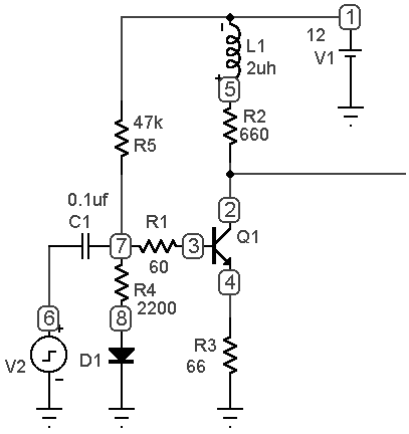
If we ignore Cfeedback (Ccb) then the transistor will Beta limit while trying to discharge a high capacitance load. With a base current of 1.8mA and a Beta of 100 then the collector current limit is about 180mA. Current from Rc and current from Cload combine to equal the 180mA limit. Current IRc is in the range of 0 to 20mA depending on Vout. The slew rate is 180mA / 32.7pF = 5500v/uS or 5.5V/nS at hi Vout and 160/32.7 = 4.89V/ns at low Vout. It takes 29nS to move from 10% to 90% or 160 volts. Which corresponds to about 17mHz. The problem is we chose the Beta at 3mHz not 17mHz. We need to go back and try another iteration.

This time choose a Beta of 30 at 4mHz. The Ic max is not 1.8mA X 30 = 54mA. Take away 10ma for IRc and 44mA is left to move Cload. The slew rate is 44mA/32.7pF = 1345V/uS or about 120ns for an 10% to 90% swing. This corresponds well to the 4mHz that we chose for the Beta frequency.

It can be seen that with only 30pf of load the beta limit is <u>not</u> the limiting factor! It will take approximately 60pf to get into Beta limiting.

Collector peaking

At D.C. the gain is R2/R3. At high frequencies the gain is (R2+L1)/R3. One method to determine the value of L1 is to first find the frequency where the gain has been reduced by 20%. Then find an inductor where's impedance would increase the collector impedance by 20% at the same frequency.



The method I usually use it to insert a variable inductor in place of L1. Adjust the inductance for optimal response. Measure the variable inductor and then substitute an appropriate fixed inductor. This method is known as "guess a value and try it".

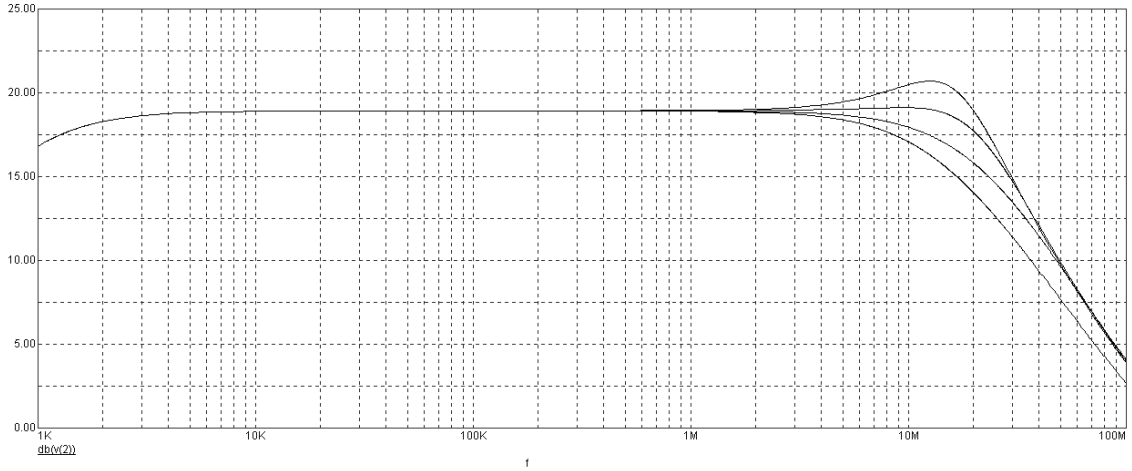
$$L1 = \frac{1}{4\pi^2 \bullet fc^2 \bullet Cc}$$

Cc is the total of all capacitance found on the collector of Q1.

Hopefully you can see that the above formula is derived from the resonant LC formula.

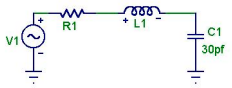
$$fc = \frac{1}{2\pi\sqrt{L1 \bullet Cc}}$$

Why use the guess method when there are formulas? The value of Cc is generally not known or only a guess its self. The high frequency role off point may be a combination of several factors and not just a matter of capacitor loading. The high frequency role off point may be a guess. Some of us work in labs with out the beast of test equipment.

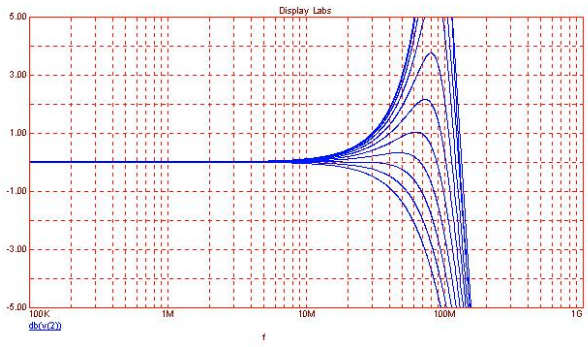


The four different curves are for different values of L1. 0uh, 2uh, 4uh, 6uh

Series peaking



Like it or not there is a RCL circuit on the output of all video amplifiers. Capacitor C1 is the load (cathode) plus all stray capacitance. Coil L1 is a combination of two/three things. Wire inductance and PCD trace inductance add to form the minimum inductance. Often this is not enough inductance to series peak a video amplifier so a small inductor is add to the output. Resistor R1 is also a combination of two factors. The output impedance if the video amplifier is the least resistance. A separate resistor needs to be added to the output of the video amplifier. R1,L1 and C1 represent the total of all Rs, Ls and Cs.



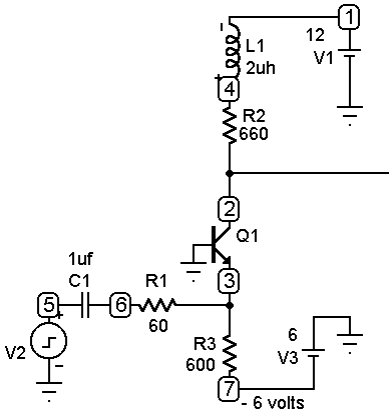
There is a formula for series peaking inductance and resistance. I will not present the formula here because the value of capacitance is not known accurately. The output impedance of the amplifier (at role off frequency) is probably not known. The trace inductance is only a guess. Why bother with the formula? The LC must be set to resonate at the frequency where the gain of the amplifier roles off. The value of C can not be changed so L1 must be tuned to the correct frequency. The value of R is set to dampen the resonance. The graph shows 10 different values for R1. When R1 is too large it forms and RC low pass filter. If R1 is too small the LC rings uncontrolled. The output frequency response is over peaked.

Resistor R1 has a secondary purpose. Tube arcs protection is very important. Any value of resistance and inductance will limit arc current into the video amp.

Frequency: $F = \frac{1}{2\pi\sqrt{LC}}$ solve for L: $L = \frac{1}{4\pi^2 F^2 C}$

Grounded Base Amplifier

The Miller effect has such a dominate effect on the speed of an amplifier that it is important to choose an amplifier topology that reduces it's effect. Transistor Q1 has a gain of 10. As stated earlier, this would multiply the Ccb effect by a factor of 11 times. The base is at ground (or an A.C. ground). This stops the feedback path from output to input normally associated with Ccb.

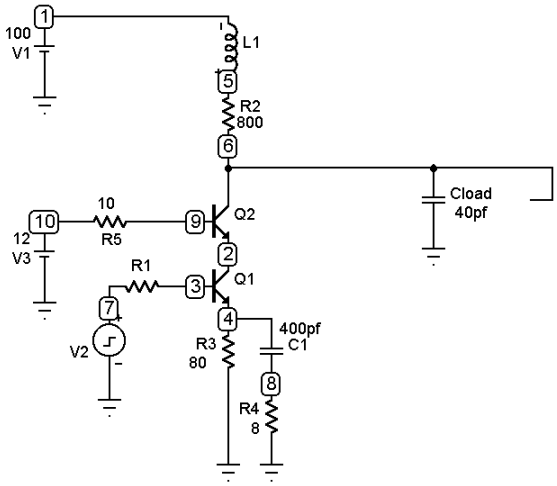


Grounded base amplifiers are not current amplifiers. There is no high impedance point. The input impedance is only 60 ohms, set by R1.

Are all the effects of Ccb removed? **NO** The Ccb still appears as loading on the collector of Q1. Thankfully Ccb current is not driving the base of Q1.

Cascode

Transistor Q2 is operated in the grounded base configuration, which does not have a Ccb feedback effect. The collector base capacitance appears from collector to ground and does not have a multiplication of 1+Vgain.



Transistor Q1 is also operated in a mode that reduces the Ccb effect. Node 9 is a 12 volts supply. Node 2 is at about 11.3 volts and appears much like a voltage supply. There is very little A.C. signal at node 2. The input signal is at node 7, 3 and 4. This leaves Q1 operating in the emitter flower mode. As stated earlier; the Ccb effect of an emitter flower is multiplied by only one.

⇒Why R5? We just learned that a grounded base amplifier is fast. Why slow down the amplifier with base resistance?

There are two functions of a base resistor for Q2. This type of amplifier is being pushed to have more gain at high frequencies by the peeking capacitor C1 and inductor L1. At the same time the h_{FE} of Q2 is dropping because of f_T. The two effects collide and cause instability and possible oscillation. Resistor R5 roles off the amplifier gain at a point higher than its operating range. It is hard to see 300mhz oscillation in a video amplifier using a 100mhz oscilloscope.

The second reason for base resistance in the output stage of a video amplifier transistor is for CRT tube arc protection. Five to ten ohms of base resistance reduces the base current under arc conditions.

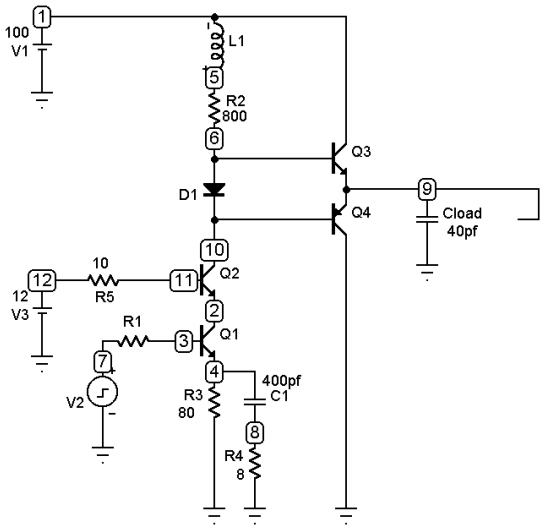
Transistor Q2 will have a longer and happier life with base resistance.

⇒Why R4? It is obvious that R2 and Cload are compensated for by R2 and C1. Why limit the effect of C1with R4?

Generally I try to keep R4 in the range of 1/5 to 1/10 of R3. Once again C1 (peeking capacitor) pushes the gain and phase upward while capacitance and f_T causes the gain and phase to drop. If the peeking capacitor is allowed to push the gain up uncontrolled there is likely to be instability and oscillation.

Cascode Emitter Flower

This circuit employs a buffer to isolate the capacitance load from the collector of Q2. The buffer only improves the speed if Cload is larger than the added capacitance of Q3 + Q4! In a monochrome CRT monitor where there is a direct connection from video amplifier to CRT cathode Cload may be too small to justify the buffer stage. Color monitors have additional circuitry added between video amp and cathode. The Cload is large and emitter flower buffers are common.

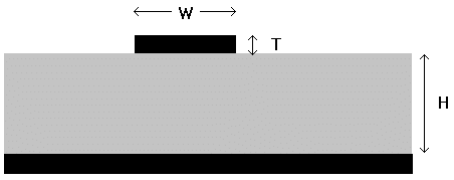


1.) Minimize the capacitance load on Q2 collector.
2.) Ic of Q3 and Q4 are due only to Cload charging current. They do not have load resistor current. Their full current is delivered to the load.
3.) Q3 and Q4 heatsinks are connected to supply and ground and do not add capacitance.
4.) Cload charging current is not limited by R2. Current from R2 is multiplied by h_{FE} of Q3.
5.) Cload charging current does not pass through Q2 thus minimizing beta limiting.

PCB effects

As video speeds get into the RF region the printed circuit board becomes a major part of the design. PCB traces add **Capacitance**, **Inductance**, **Delay** and possible **Reflections** to signals.

For the formulas below we define a PCB as folows:



Trace width and thickness are **W** and **T**. PCB thickness is **H**.
The dielectric coefficient (**d**) of the insulating material lies in the 2 to 5 range.
d ≈ FR4 fiberglass = 4.7 G-10 fiberglass = 5.0 to 5.3
T ≈ 0.0015" for 1 oz. Cu or T ≈ 0.0030" for 2 oz. Cu
H ≈ 0.062" or 0.031"

Trace Capacitance
Printed circuit trace capacitance runs around 1.67pF per inch. It is very typical to find 1 to 3pF on most nodes.

$$Co = \frac{0.67(d+1.14)}{Ln\left(\frac{5.98H}{0.8W+T}\right)}$$

1.67pF/inch

pF/inch

Trace inductance
At just above the video rate inductors and even transformers are routinely built using PCB traces!
Typically 9 to 10nH per inch

$$Lo = Ln\left(\frac{5.98H}{0.8W+T}\right)$$

nH/inch

Delay
It is of interest that the propagation delay of the line is dependent only on the dielectric constant and is not a function of the width or spacing.
1.3ns/foot

$$tpd = 1.017\sqrt{0.475d + 0.67}$$

ns/ft

The above example is for a trace with out capacitance loading. If the far end of the trace is connected to a transistor with capacitance then the delay is larger. Cl= load cap. Co= cap. of trace

$$increase = \sqrt{1+\frac{Cl}{Co}}$$

Delay with Loading
If a trace having a delay of 1.77ns/ft and a length of 2 inches resulting in a capacitance of 3.5pF, is terminated in a load of 2pF the resulting delay is 2.21ns/ft.

$$tpd = 1.017\sqrt{0.475d + 0.67} \bullet \sqrt{1+\frac{Cl}{Co}}$$

$$tpd = 1.77ns/ft \bullet \sqrt{1+\frac{2}{3.5}} = 2.21ns/ft$$

Stripline Impedance
Impedance of a stripline. If a 75Ω video needs to move across a PCB with our reflections then a stripline should be used.
75 Ω ≈ 0.062" board, one ounce Cu, 0.100 trace width
50 Ω ≈ 0.062" board, one ounce Cu, 0.049 trace width

$$Zo = \frac{87}{\sqrt{d+1.41}} Ln\left(\frac{5.98H}{0.8W+T}\right)$$

ohms

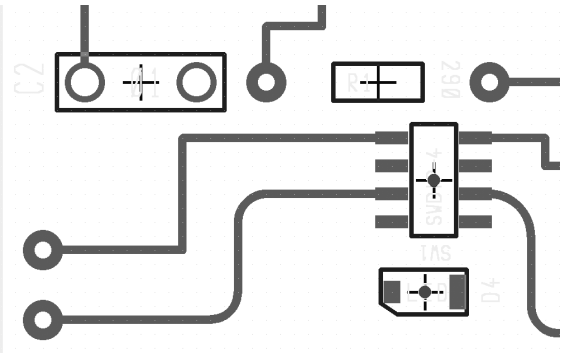
Now we are armed with many formulas. What can we do with them?

Transmission Line

A transmission line (either in coax or as a strip line in a PCB) is a way of moving a signal over a distance with our distortion. The maximum distance that a signal should be moved with out a transmission line is the rise time of the signal divided by twice the propagation delay of the line.

$$L\max \le \frac{tr}{2td}$$

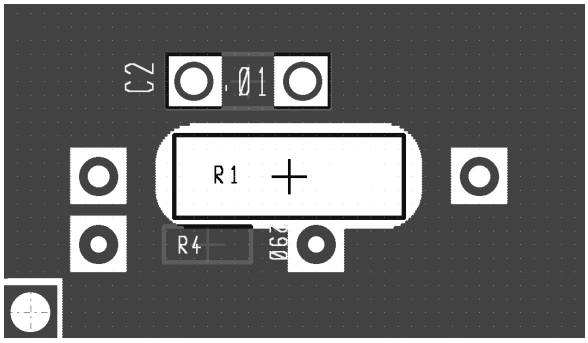
A video signal with a rise time of 1.7ns should need a transmission line with a length over 6 inches. Video boards rarely have any traces 6 inches long. With that logic it looks like we will never need to make a strip line. **Wrong!** The video DAC in the computer is probably three feet away from the video board in the monitor. The transmission line should not end at the back of the monitor. It should not end at the edge of the video board. It must continue with 75 ohms impedance



across the PCB right up to the video pre-amp and the termination resistor.

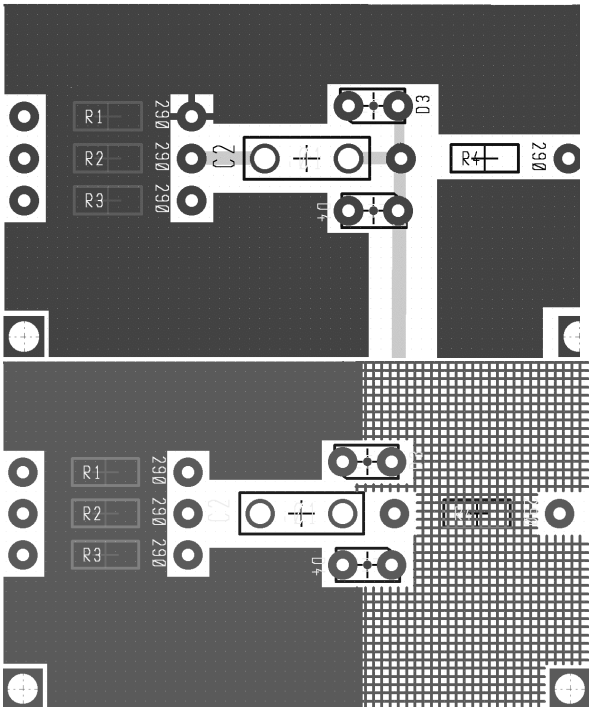
In high speed strip lines, the shape of the trace is important. The impedance of the sharp corners causes a 7.5% reflection. It is a good idea to have smooth, rounded lines and constant line widths.

Capacitance



It was found that there is a large amount of capacitance between power resistor R1 and the ground plane. The ground is removed under the resistor to reduce the stray capacitance.

Resistor R1 is the output of the video amplifier. It has also been found that during tube ark conditions the voltage on R1 gets very high. A spark jumps through the side of R1 into the ground plane cracking the resistor's insulation. The spark builds up a path of carbon leaving a conductive path from R1 to ground. If voltages can exceed 1,000 volts then it is a good idea to clear out the ground plane under carbon film and metal film resistors!



In this printed circuit board example the dark color is the topside ground plane. The light color trace is the bottom side traces. There is a signal that passes through R2, C2, D3, D4 and R4. The ground plane has been cleared out around the traces in an attempt to reduce trace capacitance.

Care must be taken to keep the ground plane intact.

The second example shows a ground planes with a crosshatch pattern in the sensitive aria. In this example the trace to ground capacitance is reduced to 50%. I used 0.007" traces set at 0.020" spacing that should have resulted in a 58% fill. The fill factor is typically 50%. Any other amounts of fill can be used (25% or 10%).

Delay

It this paper was about digital signals then at this point there would be a large section on propagation delay and the importance of matching delays across a digital board. In the analog world it is generally not necessary to match the delays in several data lines with that of a clock signal. The only signals that I can think of that should have identical delays are the R, G, B video lines. The delay from the back of the monitor, through the pre-amp, power amp and up to the neck of the CRT should be kept close. Differing amounts of delay in the three video signals will cause a distortion that looks like horizontal miss-convergence.

Series Shunt

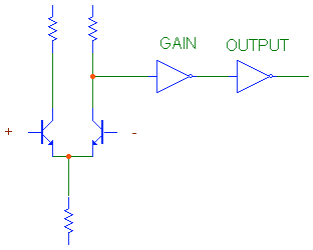
This is a type of amplifier!

Current Feedback Amplifier

Current feedback amplifiers are typically used in high speed low gain applications like video amplifiers. They differ from OP-amps in several ways.

OP-amp

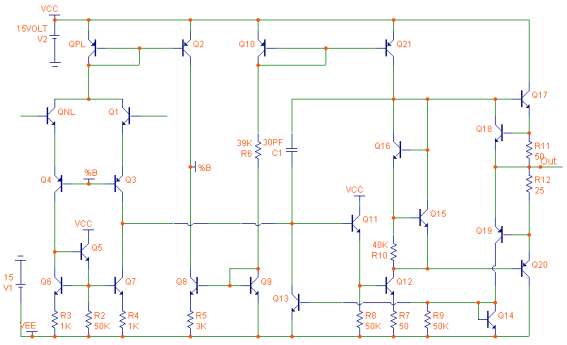
High open loop gain. There may be several gain stages.
High input impedance with symmetrical properties.



The inputs are optimized for high input impedance, low differential voltage and maximum gain. The input transistors are operating at maximum gain. To increase the input impedance the input transistors may be Darlington.

Input offset voltage is small because the input transistors are identical.

The delay through the differential input stage, through one or more gain stages followed by the output stage is long.

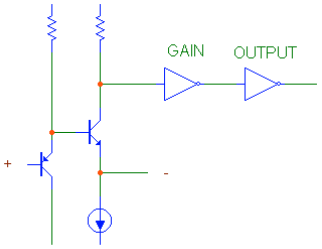


ua741

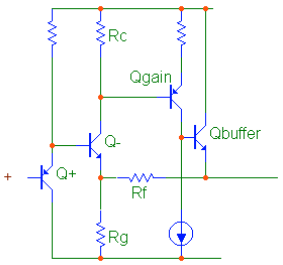
Current Feedback Amp.

Low open loop gain.

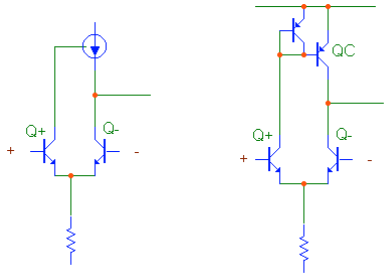
The positive input is high impedance.
The negative input is low impedance.



The + input is configured as an emitter follower which has unity gain and thus less Miller capacitance.
The – input is always connected back to the output through a low value resistor.
The input offset voltage is dependant on the gain setting.
The feedback path does not include the first transistor. The gain and output stages are simple and short. If feedback is to be used in high speed applications, the delay through the amplifier must be small.

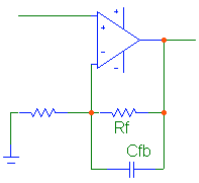


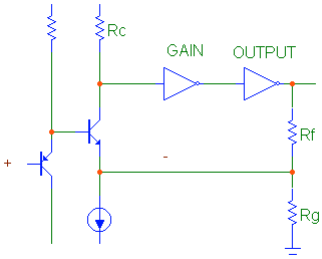
Q+ and Qbuffer are operating with a Vgain of one so they are fast. The output load capacitance does not appear on the collector of Qgain thanks to Qbuffer. The speed of Q- is set by Rg//Rf.



If the + input is increasing in voltage then Q+ will pull more collector current causing the current source QC to turn on harder. At the same time QC (the current source) is pulling up harder, Q- will be drawing less collector current thus releasing the output. The voltage gain of the input stage approaches the maximum gain of Q+ or Q- multiplied by the maximum gain of QC. The Miller effect caused by Ccb is multiplied by 1+Vgain. The speed of an OP-amp is determined by its closed loop gain.

Using a OP-amp Cfb is used to roll off high frequencies.





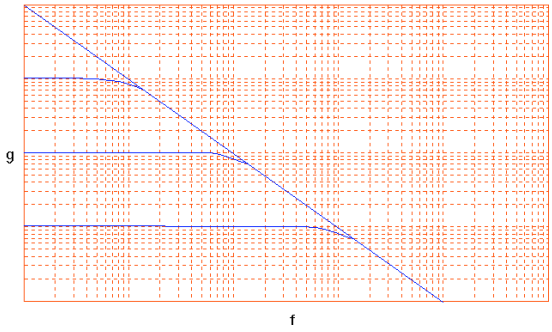
The gain of the second transistor is set by the ratio of Rc over the emitter resistance (Rf // Rg). If Rf is constant, the gain is set by Rg. A small value of Rg results in a higher voltage gain and a faster input stage. The results is the amplifier's bandwidth is almost independent of the gain setting.

$$gain = 1 + \frac{Rf}{Rg}$$

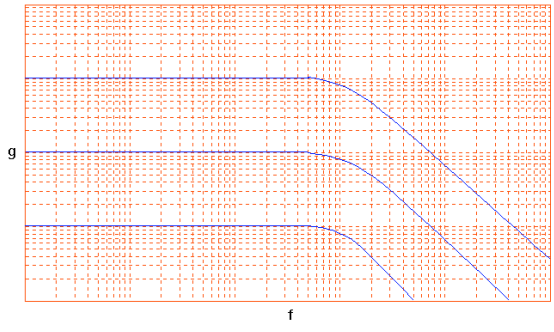
To slow the amplifier increase the impediance of Rf//Rg. To speed up the amplifier decrease the impediance at the negative input.
Never connect a capacitor from the negative input to output of a current feedback amplifier! It will cause instability.

To slow down a current feedback amplifier increase the value of Rg.

A small amount of peaking can be achived by placing a small capacitor from the negative input to ground.



Typical voltage gain vs. frequency of an OP-amp. High gain amplifier configurations are slow.



Typical voltage gain vs. frequency of a current feedback amplifier. Where Rf is constant and Rg is varied to set the gain.

SCATTERING PARAMETERS S-Parameter

S-parameters are often used to describe high frequency networks (amplifiers, filters & transmission lines). They are found in data sheets for video amplifiers, RF amplifiers and high speed transistors. S-parameters are measurements of incident and reflected current, voltages or power between the source, amplifier and load as well as transmission gain/losses. They can be expressed in absolute values or in db, in voltage or power. S11 and S12 are related to VSWR. The parameters for a two-port network are defined as:

S11=Input Return Loss

$$S11 = \sqrt{\frac{power\_reflected\_from\_input\_port}{power\_available\_at\_input\_port}} = \frac{voltage\_reflected\_from\_input\_Port}{voltage\_available\_at\_input\_port}$$

S11 is related to VSWR.

$$VSWR = \frac{|1+S11|}{|1-S11|} \qquad \text{Return\_loss} = 20\log\left(\frac{VSWR+1}{VSWR-1}\right) = 20LOG(S11)$$

$VSWR = \left|\frac{Zi}{Zs}\right|$ where Zi is the amplifier input impedance and Zs is the source impedance.

The ideal VSWR is 1. A typical VSWR is 1.5 for RF amplifiers. A S11 of 25db is also good.

S12 Reverse Transmission Loss or Isolation

Is a measure of how much signal injected into the output of an amplifier makes it to the input of the amplifier.

$$S12 = \sqrt{reverse\_power\_gain} = reverse\_voltage\_gain$$

S21 Forward Gain or Loss

The device under test can have voltage gain like an amplifier or voltage loss (attenuation).

$$S21 = \sqrt{power\_gain} = voltage\_gain = \frac{Vout}{Vin}$$

S22 Output Return Loss

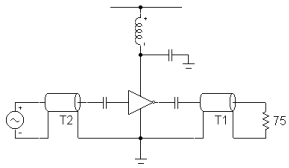
$$S22 = \sqrt{\frac{power\_reflected\_from\_output\_port}{power\_available\_from\_output\_port}} = \frac{voltage\_reflected\_from\_output\_port}{voltage\_available\_from\_output\_port}$$

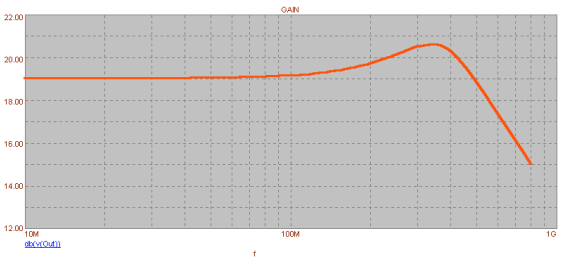
$$VSWR = \frac{|1+S22|}{|1-S22|}$$

$$Pin = \frac{Vin^2}{Zin} \qquad Pout = \frac{Vout^2}{Zout}$$

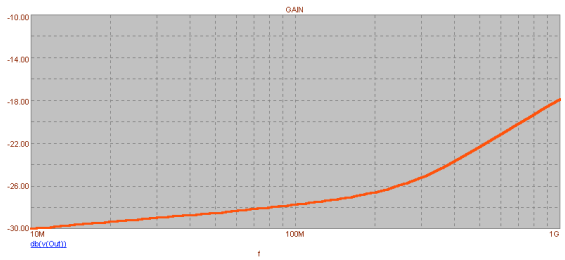
Review:

This amplifier has an input and output impedance of 75 ohms with a voltage gain of 10X or 20db. These values are dependent on frequency as seen in the graphs.

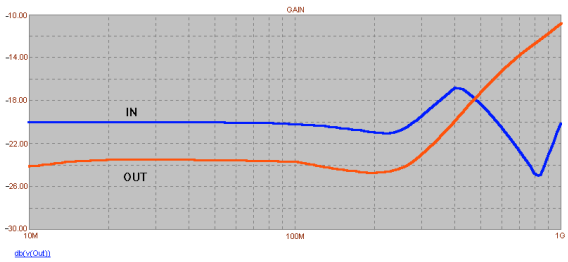




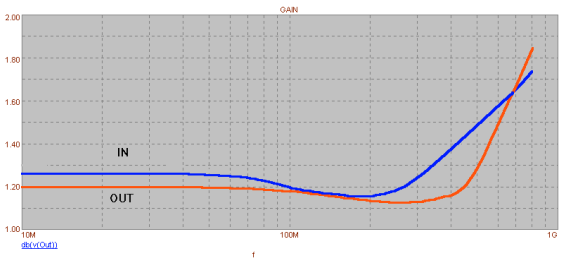
S21 The voltage gain is 19db, peaks at 20.5 and falls off to 15db at 800mhz.



S12 The reverse feed through is much worse at high frequencies.



S11 & S22
Input & output return loss from data sheet.



VSWR Input & output reflected verses frequency including PCB and connector effects.

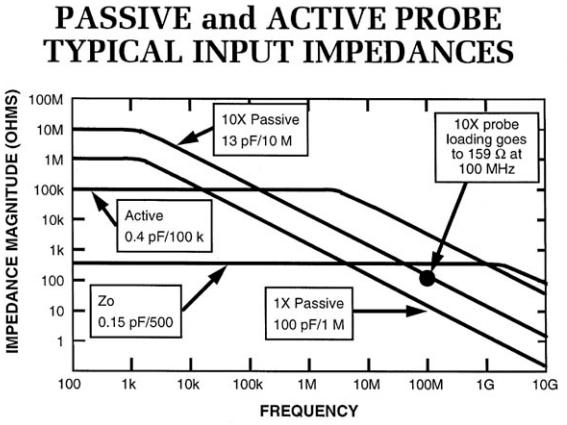
From the amplifier's data sheet: S11db=20db which is S11=0.1

Convert to VSWR: $VSWR = \frac{|1+.1|}{|1-.1|} = 1.22$ Add a connector: input VSWR=1.25

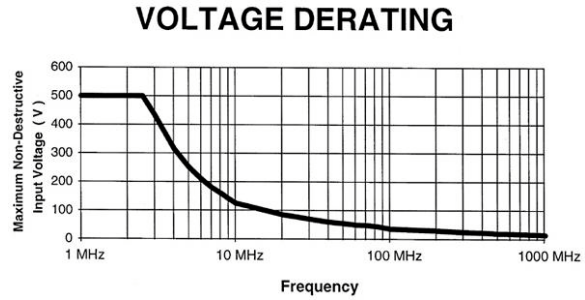
From the amplifier's data sheet: S23db=23db which is S11=0.07

Convert to VSWR: $VSWR = \frac{|1+.07|}{|1-.07|} = 1.15$ Add a connector: output VSWR=1.2

Oscilloscope Probes



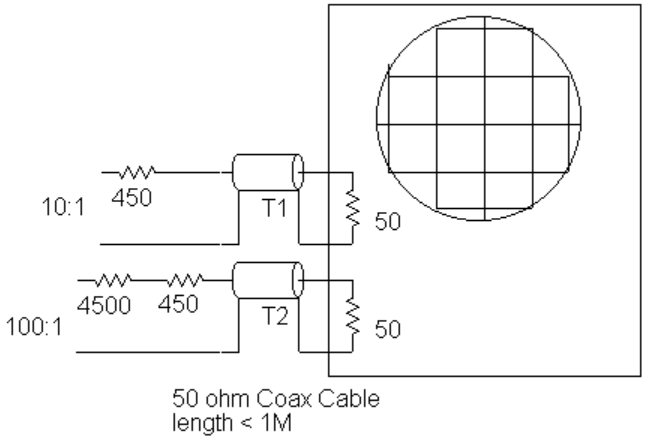
A typical oscilloscope probe has 10MΩ resistance in parallel with 12pF capacitance. That is 79Ω at 200MHz! The tube cathode capacitance is another 12pF. Stray capacitance found in the tube socked, arc protection circuitry, black level clamp, D.C. bias amp, wires and traces could add another 10pF. The normal loading of the video amplifier is 22pF. With the probe the loading increases to 34pF. The amplifier will <u>not</u> operate the same! With a 30 volt peak to peak signal there will be approximately ¼ amp of current in the oscilloscope probe! Chose your probe wisely.



The 12pf is the problem so we must find a way of looking at the video signal with out adding capacitance. There are available several low capacitance probes. They come in two types; active and passive. The active probe I have has a built in amplifier. The problem is that it can not handle high voltage signals. All probes have a problem handling high voltage signals. When you mix high voltage and high frequency the probe's A.C. plus D.C. voltage can easily be exceeded. The passive probe is 1pf and 5000 ohms. It works very will if the amplifier can handle the 5000 ohms load. This probe can not handle more than 70 volts D.C. it typically needs to be A.C. coupled to look at the cathode of a CRT.

Home made probe

Passive low capacitance probes can easy be built. The oscilloscope must be switched to 50 ohms impedance. Use a short length of <u>good</u> 50Ω coax. On the end of the coax solder a 4950 or 450 ohm resistor. Any divide by ratio can be used. Watch the power rating on the resistor. It is not uncommon to find 100 volts of bias on the cathode of a CRT tube. You may want to A.C. couple the probe by adding a D.C. blocking capacitor in series with the 4950Ω resistor. Keep all lead lengths <u>short</u>. Keep the ground lead length very short. Use a non-inductive resistor!



Many resistors will have a small amount of stray capacitance that forms a peaking capacitor. You may need to add the tiniest amount of peaking capacitor. Amateur Radio Operators commonly build high voltage sub-pf capacitors by twisting together insulated wire. The first resistor in the photo has added three twists of insulated wire held together with clear heat shrink tubing. The wire can be cut shorter to reduce the capacitance. Twisting the wire tighter will increase the capacitance. The second resistor has the two wires run in

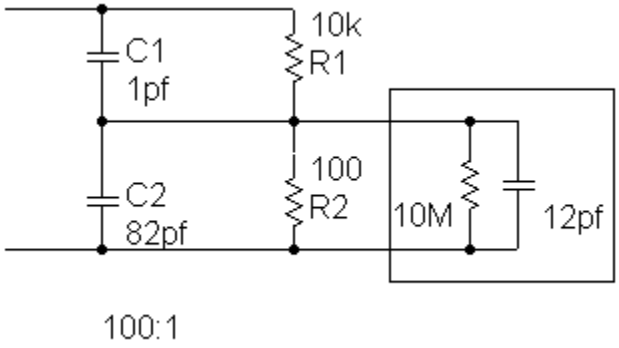
parallel inside clear tubing. The wires can be pulled back to reduce the capacitance.

Sniff the Video (no direct connection)

Another option for viewing the output of a video amplifier with out adding loading is to wrap the cathode wire around the scope probe. The wire to probe capacitance is only a fraction of a pico-farad. The results is a divide by many thousand. The gain of the scope will have to be turned up all the way. The probe is A.C. coupled! No low-frequency effects can be seen. This method is only good for looking at edges.

÷100

To get a low voltage version of what is happening at the output of a video amplifier I some time solder a 100:1 divider onto the amplifier. Remember the leads must be very short. To measure the rise and fall time of the amplifier an A.C. only divider can be made with two capacitors. If the D.C. level in important then resistors must be added. The 10MΩ/12pf is the oscilloscope probe. C1,C2,R1 and R2 are soldered onto the amplifier.



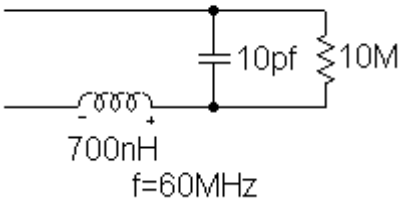
100:1

Ground Lead

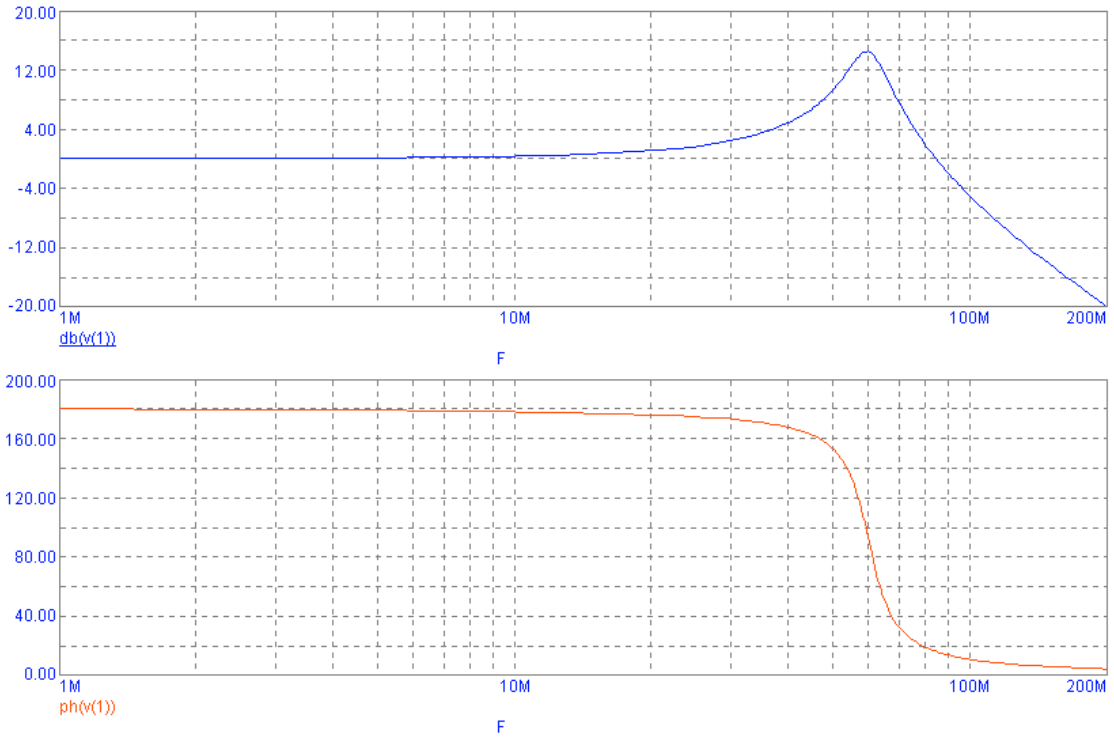
First throw away the alligator clip ground wire! A 10X oscilloscope probe adds 10pF and 10MΩ which might not cause trouble. A six inch ground lead has about 700nH of inductance.

$$f = \frac{1}{2\pi\sqrt{lc}} = \frac{1}{2\pi\sqrt{700nH \bullet 10\,pf}} = 60MHz$$

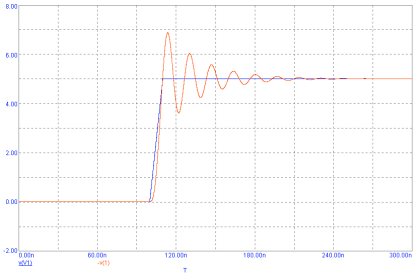
You have just inserted a LC resonant circuit into your amplifier (or should I say your oscillator)!



If the point you are looking at has fast edges it will cause the LC to ring. The oscilloscope will see ring that is not there. Below is the frequency and phase response of a 10X probe with a 6" ground lead.



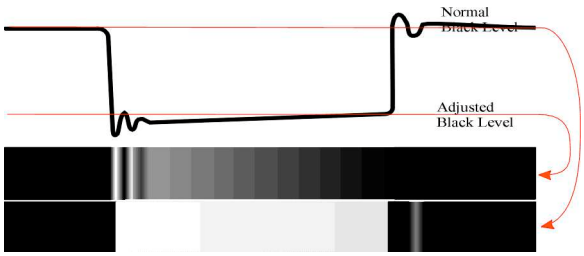
Would you use a probe with this frequency response? Have you seen this ring before?



The actual ring is different than this spice model. The ground lead is more complicated than a simple inductor and the capacitance is also complex. Move the path of the ground lead an inch and the look of the ring will change.

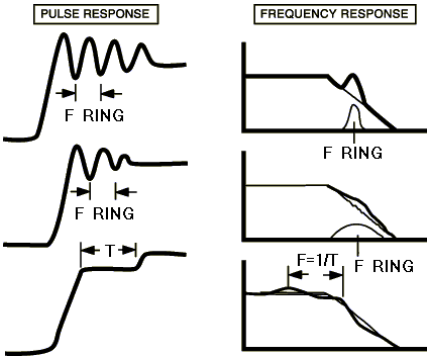
I make or buy small loops of wire (or spring wire) that both hold the probe in place and grounds the probe. The wire is soldered into the PCB at a ground location.

Do not trust your oscilloscope! There are too many factors that have to be just right. The important thing is to trust your eyes. That is how the end customer will judge the product. The output of a video amplifier that drives a CRT tube has a high level for black and a low level for white. Normally the grid bias is set so that the high level makes black. 10% video ringing is almost impossible to see.

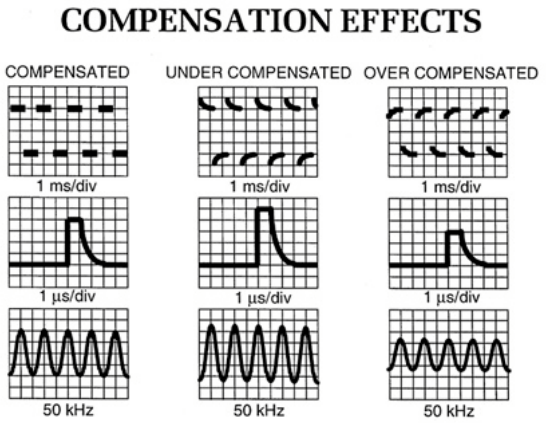


To see the details of the video set the bias very black; so just the tips of video will be beyond the black level. Turn the room lights are turned out to see the imperfections in the video level. In the above example; ringing becomes apparent. Notice the slope to the video. It shows a low frequency response problem.

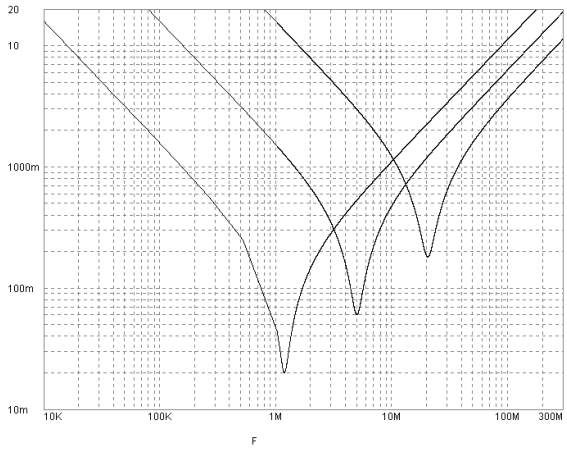
Say something here about step function verses frequency response. Try to make it sound like one of us knows what we are talking about! I don't know what to say.



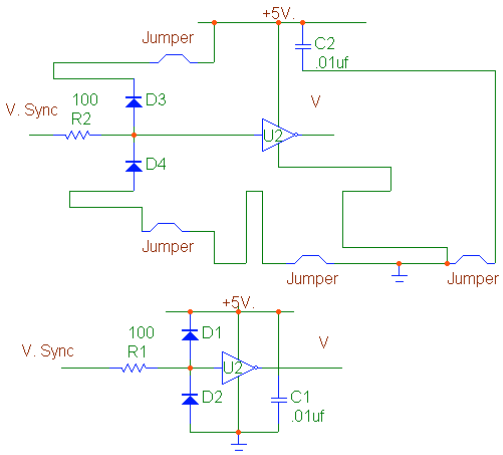
Probe calibration



Impedance of three capacitors 1uf, 0.1uf and 0.01uf from the same vender and same type.

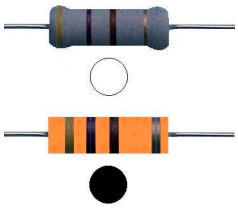


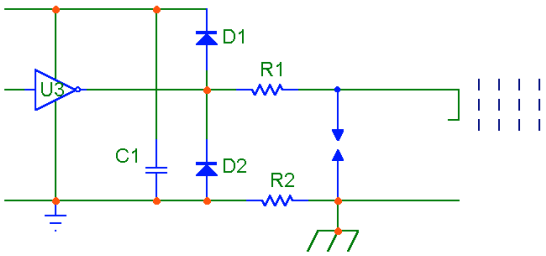
A few years ago a major monitor company came to DL with a monitor that lost vertical sync after any hard tube arc. The repair was to replace U2, the vertical sync buffer on the video board. The engineers had added resistors and diodes to the sync lines with some effect. Adding MOVs and small capacitors did not help. They tried adding diodes on both sides of the input resistor with out effect.



Here is the schematic, <u>as traced from the printed circuit board</u>. I hoping "a picture is worth a thousand words".

A typical





HORIZONTAL SYNC

##########

VERTICAL SYNC

##########

BACK PORCH

Back porch clamping pulses are created by detecting the trailing edge of sync. The width of this pulse should be a little shorter than the back porch.

<u>VIDEO</u>

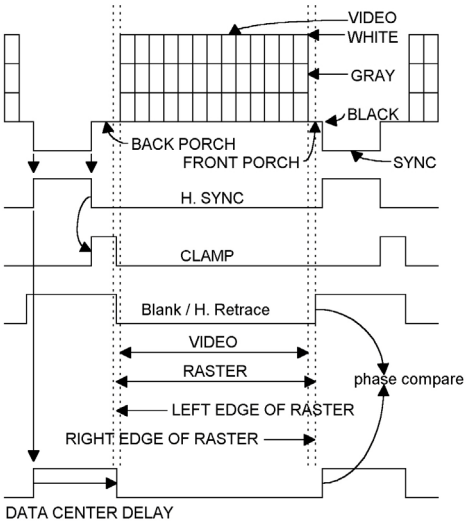
The video board is in the very back of the monitor. It contains the three video power amplifiers, a three channel preamp and the sync processing circuits.

Data Centering Delay

The green video may or may not have the sync signal. Red and Blue video usually does not have sync.

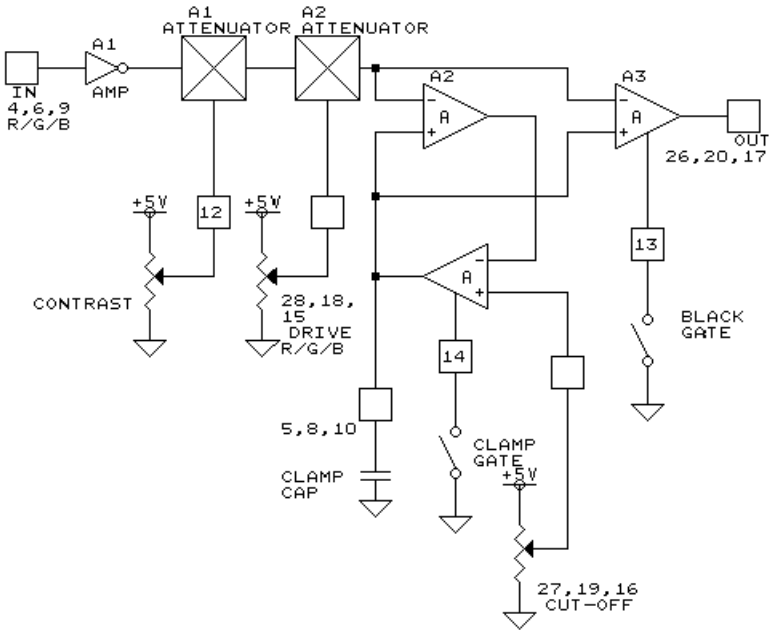
Shortly after the rising edge of composite sync the "Clamp Pulse" starts. The clamp pulse must be shorter than the video back porch.

The falling edge of composite sync starts the "Data Centering Delay". The end of the delay coincides with the left hand edge of the raster.



LM1205 GENERAL DESCRIPTION

The LM1205 is a wide band video amplifier intended for super VGA resolution color monitors. The LM1205 contains three matched video amplifiers, a common contrast control, a blanking function, and back porch clamp.

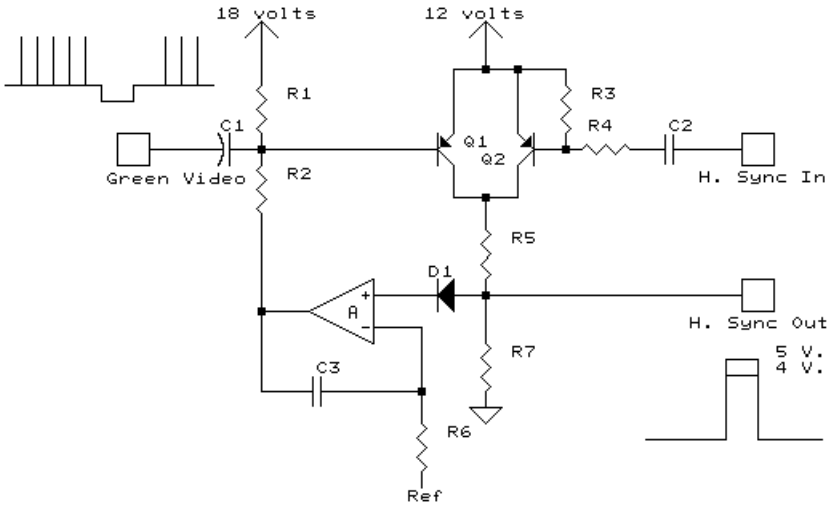


The above diagram shows part of the inside of the LM1205. The contrast control changes the gain of all three channels (R/G/B). The difference in gain of each gun is compensated for by gain adjustments for each amplifier outside of that of the contrast control. The cut off control sets the bias level for each channel.

LAY OUT

The LM1205 must be close to high frequency bypass capacitors which quickly return RF energy to ground. Component placement around the LM1205 is very critical in order to insure stability.

SYNC SEPARATOR



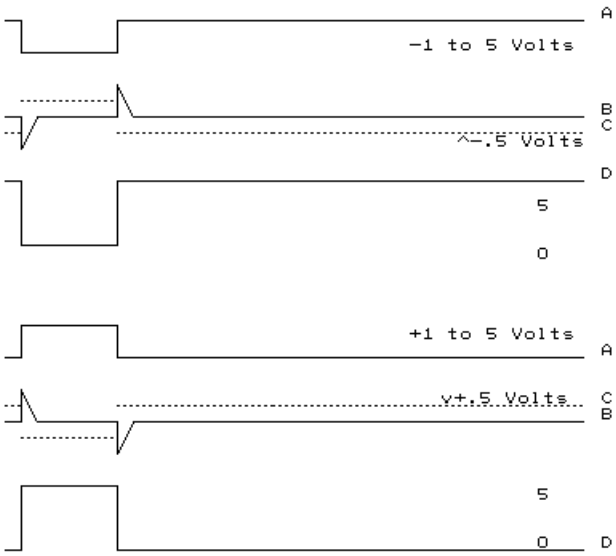
The sync separator will extract sync from composite video if no external sync is present. The external sync input overrides any sync on green video.

Video containing sync is A.C. coupled to Q1-base. The op-amplifier looks at the peak out put sync signal. The amplifier adjusts the bias on Q1 such that Q1 turns on during sync but dues not saturate. This leaves Q1 operating in the linear region. The sync out signal has a 4 volt peak level.

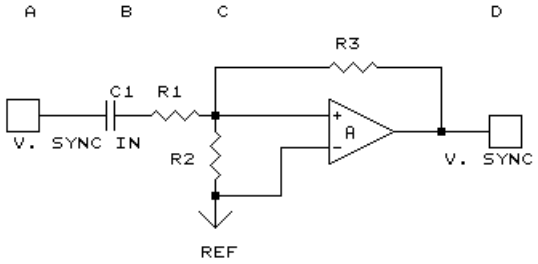
If sync comes from the sync input it will over ride any sync that might be present on video. External sync will drive Q2 into saturation during the negative portion of sync. Through the divider R5 and R7 the sync out will have a peak to peak voltage of 5 volts. This will be greater than the reference voltage on the op-amplifier. The op-amplifier will allow the base of Q1 to go positive above it's emitter causing Q1 to not operate.

V. SYNC

The vertical sync input must respond to a 1 to 5 volt signal that may not be will referenced to ground. The ground problem is solved by A.C. coupling. Noise immunity is gained by positive feedback. The slicing point is set to about .5 volts away from the average level of the signal. In the diagram below the slicing point moves by 1 volt depending on the polarity of the signal.



R3 sets the positive feedback. R2 sets bias. R1 sets the gain. C1 removes the D.C. component of the incoming V. sync.



Simplified diagram if the vertical input amplifier.

BRIGHTNESS CONTROL

####################

CONTRAST CONTROL

################

CLAMP

#############

BLANK GATE

################

If application is to use video blanking at the preamp, the blank signal is applied to Pin 13.

BLANK COMPARATOR

################

Blank Comparator (Cutoff) control input. Accepts 0-4V input, controls blanking pedestal by setting dc level as a reference for all 3 channels. Adjusting Cutoff will shift all waveforms up or down.

POWER VIDEO AMPLIFIER

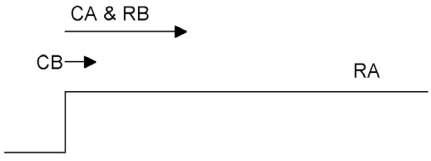
The video output stage is made of a hybrid amplifier. The LM2419 is a three channel wide band, large signal high slew rate amplifier. The output is capable if a 40 volt swing in less than 7 nS. The gain is approximately 15.

Oscillation is hard to detect. The amplifier is capable of oscillations frequency higher than some oscilloscope can detect.

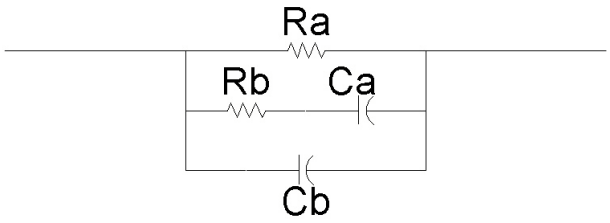
When viewing the output of the amplifier use a 100:1 low capacitance probe (1.5pF). Placing 10pF from a 10:1 probe on; the amplifier will slow down it's response.

PEAKING

Two types of video peaking are used to get the best video response. High band peaking is used to set the response of the first pixel or a single pixel. The mid-band peaking sets the response of pixels 2 through about 7.



Between the preamp and the video output amplifier are the video peaking components. At low frequency CA, CB and RB do not effect the circuit. The drive for low frequency signals, is sent by RA. At a high frequency determined by CB, the amount of drive is set by RA and RB in parallel. At a very high frequency CB increases the drive even more.

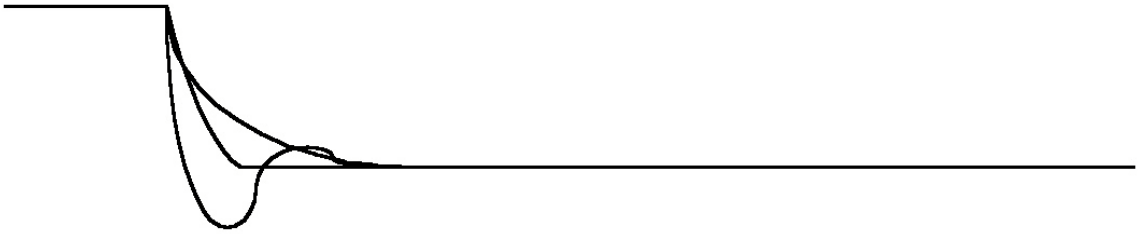


We have experience that the value of CB will be the same for all video power amplifiers with the same date code. Amplifiers made at a different time may require a different value.

HIGH END PEAKING

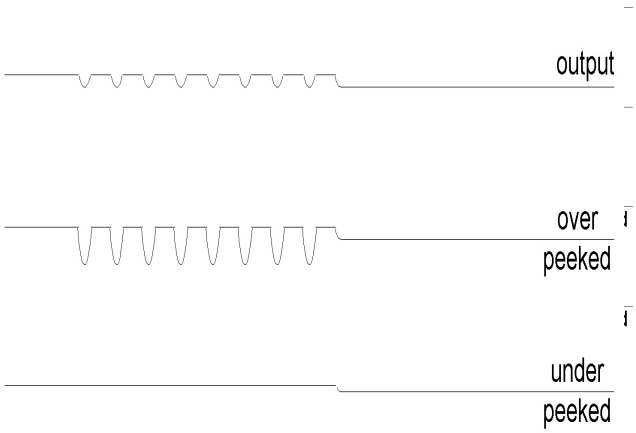
There are three video preamplifiers and three power amplifiers each with it's own frequency response at the very high end. There is no way to get three perfectly matched preamps and three matched power amplifiers. On the video board there are trimmer

capacitors to set the very high end frequency response for each channel.



If the back ground is set for black then the variations is high end frequency response is hard to see. In the black ground is set very black then the differences is frequency response is very noticeable.

The video generator produces a large white block and a block of every other pixel on next to each other. The vertical line on the right would show the frequency of the large white block. The vertical line on the right shows the frequency of the every other pixel region. If the color balance is done correctly then the white block will look white. If the high frequency peaking is not adjusted correctly then there will be a color shift in the high frequency part if the test pattern. If G2 is adjusted so only the tips of video can bee seen then the differences in video will be easy seen. When G2 is moved blacker the slowest channel of video will disappear first. When G2 is further reduced only the over peaked channel appears.



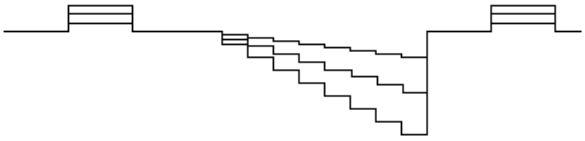
The most accurate way to set high frequency peaking is to (after color balance) set G2 so that the white block is about 1/4 as bright. Contrast should be set for 2/3 of maximum. Adjust the high frequency capacitors on the video board for the same shade of color in the high frequency block.

This diagram shows what happens when G2 is set to cover up most of the video.

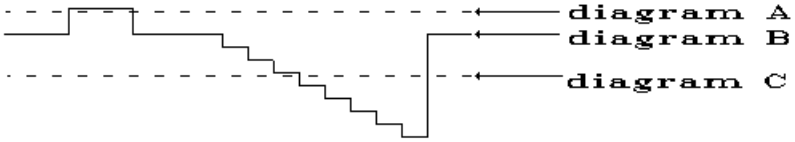
CONTRAST & BRIGHTNESS

The contrast and brightness controls plug into the video board and adjust how the picture looks on the screen. The words "contrast" and "brightness" come from the television industry and are misnamed. In a television the "contrast" control does change the distance from black to white and the 'brightness' appears to change how bright the picture is. On a non-gray scale monitor, where the picture is black or white with no gray, the two controls are nearly impossible to tell apart. Over most the range they will do the same job. In critical applications like a gray scale monitor the controls function much differently then the names imply.

Below is the video wave form on the cathode of the CRT. The highest portion of the wave form represents the blackest part of the picture. As the wave goes lower the picture gets brighter. The three lines represent three different settings of the contrast control. The black level (at the top) stays stationary while the bright portions of the picture change intensity with the contrast control. If the user wants to make the picture 'brighter' or 'dimmer' then the contrast control should be adjusted not the brightness control.

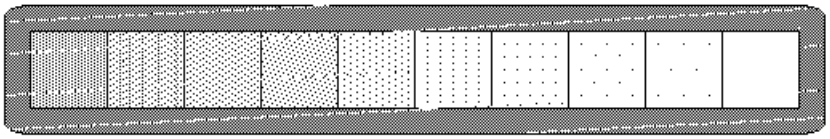


The 'brightness' control refers to the intensity of the black part of the picture.

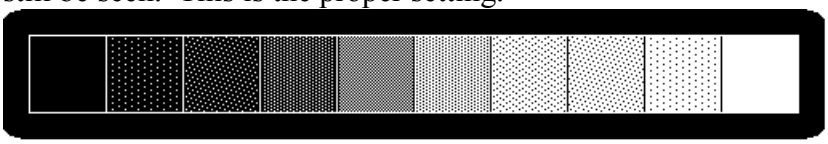


The brightness control should only be used to set the background to just disappear. This control should not be used to change the overall brightness. The next diagrams refer to three possible levels of brightness settings.

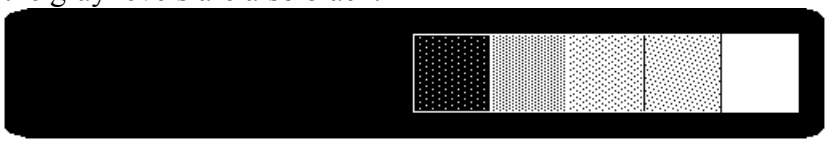
In A the background appears gray. Blacks are not black. The retrace lines appear in the background. Picture quality is poor.



At level B the background has just disappeared. Blacks are black. Low level grays can still be seen. This is the proper setting.



Level C results in the loss of many of the low levels of gray. Black is black but half of the gray levels are also black.



REGULATORS

Three voltages are used to run the video amplifier and sync processing circuit. The 180 volts is used to set the black level. The 75 volts is used by the video power output amplifier. The 16 volts is reduced to 12 volts by the 7812 regulator for use by the LM1205.

PROTECTION

All elements of the tube have arc protection. The arc current should be returned through the arc ground, not the signal ground, back to the tube in a short direct low impedance path.

BLACK LEVEL

The three cathodes are AC coupled to the video amplifiers. The DC on each cathode is set by a cutoff amplifier and clamp diode. The value of the DC voltage is adjusted for black.

FILAMENT

The filament is powered from 9 volts floating supply. A dropping power resistor reduces the 9 volts to the 6.3 needed by the heater.