## VERTICAL POWER AMPLIFIER POWER AMPLIFIER

A vertical power amplifier is very much related to an audio power amplifier. Audio amplifiers are voltage amplifiers (voltage in voltage out). Vertical amplifiers are current amplifiers (voltage in current out). The feedback comes from a current sensing point. This is done because it takes current to get deflection.



Audio amplifier Vertical amplifier Low noise is critical. Open loop unity gain extends out to 1 to 10mhz. A small monitor may need only 0.5 amps of vertical yoke current using a 12 volt supply. Large color monitors may require 3 to 4 amps and use a 35 volt supply during vertical trace and 70 volts during retrace.

## **VOLTAGE DOUBLER**

In order to obtain sufficiently short flyback times, a voltage greater than that required during scanning must be applied to the yoke.

During vertical retrace time a large voltage is needed across the yoke to cause a fast retrace. A voltage double boosts the positive supply voltage only during vertical retrace. This way the vertical power amplifier can run from a low supply voltage when little output voltage is needed and from a high supply voltage for the short time that a high output voltage is needed. The results is 1/3 the power loss and 2 to 3 times faster retrace.

The top trace is the output voltage of the power amplifier. The second trace is the supply voltage.



ANTI-RINGING RESISTOR



Many power amplifiers have instability in the 1 to 3Mhz region. An anti-ringing resistor & capacitor dampens out oscillations. See the manufacture's data sheet for proper values. Generally the resistor is in the 1 to 5 ohm range. It is chosen to load down the amplifier at the oscillation frequency. The time constant for the RC is often in the .2 to 1uS range. The impedance of the capacitor, at the oscillation frequency, should be  $\frac{1}{2}$  to  $\frac{1}{4}$  that of the resistor.



If the value of the capacitor is too large the resistor and the amplifier will get hot.

# Vertical Damping Resistor

In many vertical amplifier designs a damping resistor is placed across the yoke. One method to determine the resistor value is to select a power resistor in the 100 to 500 ohm range and adjust the value for best results. As can be seen, too large a value of resistance leaves oscillation. Too small of a value slows the amplifier.

The second method of determining the damping resistor value involves knowing the power amplifier's gain/phase plot. The gain and phase of the resistors, capacitors and yoke inductance must also be known and plotted on the same graph. Watch for adequate gain and phase margine.



The power amplifier <u>can not</u> pull it's output all the	VsatH = 2.2V @ 3A
way to the supplies. From the data sheet there	VsatL = 0.9V (a) 3A
should be terms like 'output saturation voltage to	Ũ
ground' and 'output saturation voltage to supply'	
both measured at the peak yoke current. The total	
voltage lost to the power amplifier's saturation	Vsat = VsatH + VsatL
effect is Vsat.	Vsat = 3.1V
The voltage lost to resistive effects must be found.	Vr=(1.2Ry +1.05Rf) X Iy p-p
The yoke resistance is typically only 20% accurate.	= (1.2  X  1 + 1.05  X  10)  X  6
Current sense resistors are 5% accurate. Therefor	Iy $p-p = 6A$
use 1.2Ry and 1.05Rf to get the worst case values.	
It takes voltage to get a change in current. The	Vl = (Ly X Iy p-p)/Ts
voltage needed is a function of yoke inductance X	
yoke current peak to peak divided by the scan time.	
Vc is the voltage due to the charge of capacitor Cd.	Vc = Ly X Ts / (8X Cd)

# VERTICAL CENTERING

Most vertical amplifiers are A.C. coupled. The very nature of A.C. coupling will cause the <u>raster</u> to be centered on the screen. The video will be slightly <u>low</u> on the screen. This is because there are generally 0 to



1 blank lines under the picture and many blank lines above the video. Any current pulled from the cold side of the deflection yoke to ground will cause the video to slide up. If more range is needed then the centering circuit must be built to push and pull. One to two watts and easily be dissipate in the centering resistors.

If the D.C. blocking capacitor is extremely large then the cold side of the yoke would have no voltage movement. This is <u>not</u> the case. Several volts of signal appear on the cold side of the yoke because of the impedance if the D.C. blocking capacitor and the current sense resistor. This causes the centering current to change from top to bottom of the screen. This causes a non linearity effect that on many monitors is not corrected for. A more accurate circuit includes a current source in place of the resistors.



## D.C. VERTICAL AMPLIFIER

Because the vertical yoke is D.C. coupled the vertical centering is handled within the vertical power amplifier. Very slightly pulling up or down on either input of the power amplifier will cause a D.C. current to flow through the vertical yoke. This will make the entire picture move to a new vertical position on the tube. There is no D.C. blocking capacitor in the yoke current path. The power resistors are also saved.

## VERTICAL OSCILLATOR

# **RAMP GENERATOR**

The vertical oscillator and ramp generator are combined in one circuit.

A timing capacitor is connected to pin 13. A current source charges C13 causing a ramp. The current source is controlled by pin 12. The presents if a negative edge on pin 14 causes the ramp to reset and start over again. If no vertical sync is present on pin 14 then when the ramp reaches 6.8 volts the I.C. will generate it's own sync. Any sync pulses that appear when the ramp is less than 5.2 volts will be ignored. The quality of the timing capacitor on pin 13 is critical! This capacitor must have very good temperature stability.

Here is a example for choosing C13 and the resistors on pin 12.

Knows:

The vertical ramp starts at 2 volts and should end at 6 volts. The p-p voltage is 4 volts. The timing capacitor is .1uF.

If the minimum vertical frequency is 41Hz then the capacitor has 24m seconds to ramp 4 volts in.

4 volts \* .1uF ------ = 16.7u amps 24m seconds

Thus the current source will produce 16.7uA at the lowest vertical frequency.

If the maximum vertical frequency is 125Hz then the vertical time is only 8m seconds and the current source must deliver 50u amps.

4 volts \* .1uF ----- = 50u amps 8m seconds

The next step is to choose resistors to connect to pin 12 that will deliver the 16.7 to 50u amps needed to cover the frequency range. The voltage at pin 12 is 3.5 volts. The range of the VHOLD DAC is 0 to 5 volts. The average D.C. on the VSLOPE DAC is 2.5 volts thus the voltage across R12C is 1.5 volts. (3.5-2.5)

At the maximum vertical frequency the VHOLD DAC will be at 0 volts. There will be 3.5 volts across R12A and R12B.

R12B R12C R12A ------ + ------ = 50u amps 3.5volts 1.5volts 3.5volts

At the minimum vertical frequency the VHOLD DAC will be at 5 volts. The voltage across R12A is -1.5 volts. (3.5-5)

R12B R12C R12A ------ = 16.7u amps 3.5volts 1.5volts 1.5volts

**VERTICAL LINEARITY** LINEARITY

Vertical linearity is achieved by adjusting the vertical ramp's slope many times down the screen.

The VSLOPE DAC has a A.C. wave form on it that modifies the slope of the ramp to cause linearity corrections.

At the maximum vertical frequency and with the [vertical shape at vertical frequency maximum] set to a value that causes a 4 volt p-p signal on the VSHAPE DAC set R12C for good linearity. If the vertical frequency is reduced then the p-p voltage on the VSHAPE DAC will reduce. This is set by the [vertical shape at vertical frequency minimum] control.

#### VERTICAL SIZE

The vertical size is controlled by a variable gain amplifier. The voltage on pin 16 (0 to 5 volts) will adjust the size of the vertical ramp on pin 15 by  $\pm 20\%$ .





## VERTICAL SYNC

During the time when the vertical ramp on pin 13 is less than 5.2 volts all vertical syncs are ignored. If the ramp on pin 13 reaches 6.8 volts then the TDA8102 will create it's own vertical sync. External sync functions only when the ramp is in the 5.2 to 6.8 volt range.



# HORIZONTAL SYNC

################### VERTICAL SYNC