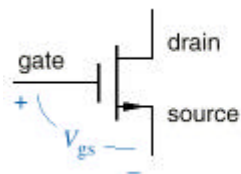


Metal-Oxide Semiconductor Field Effect Transistor



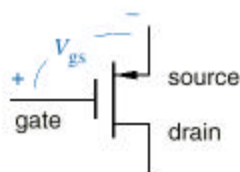
N-Channel MOS (NMOS) Transistor



Voltage-controlled resistance:
increase $V_{gs} \implies$ decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

P-Channel MOS (PMOS) Transistor



Voltage-controlled resistance:
decrease $V_{gs} \implies$ decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

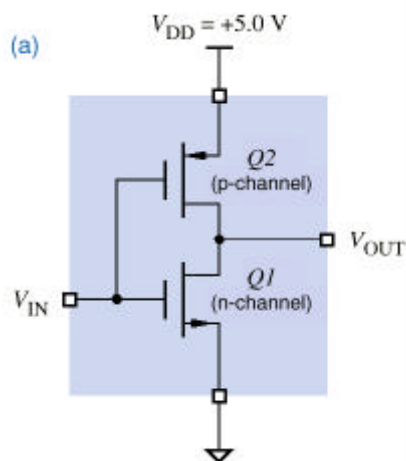
Complementary Metal-Oxide Semiconductor

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CMOS Inverter



V_{IN}	$Q1$	$Q2$	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

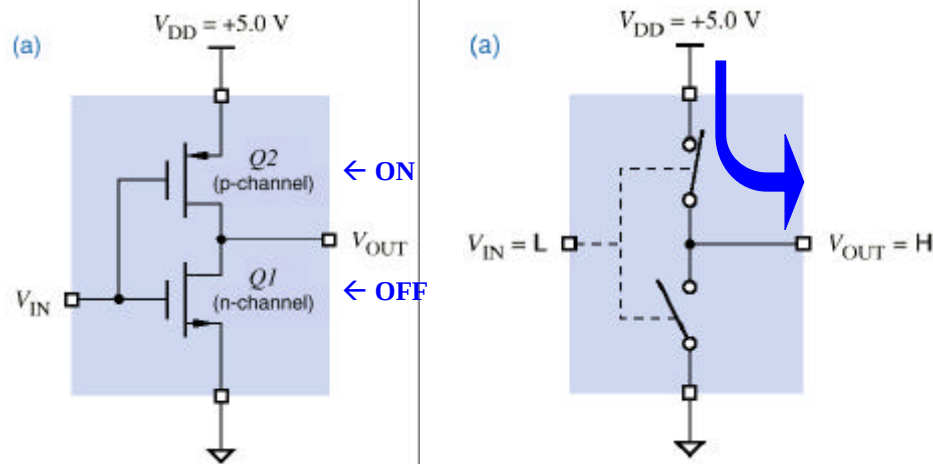


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CMOS Inverter : Low Input

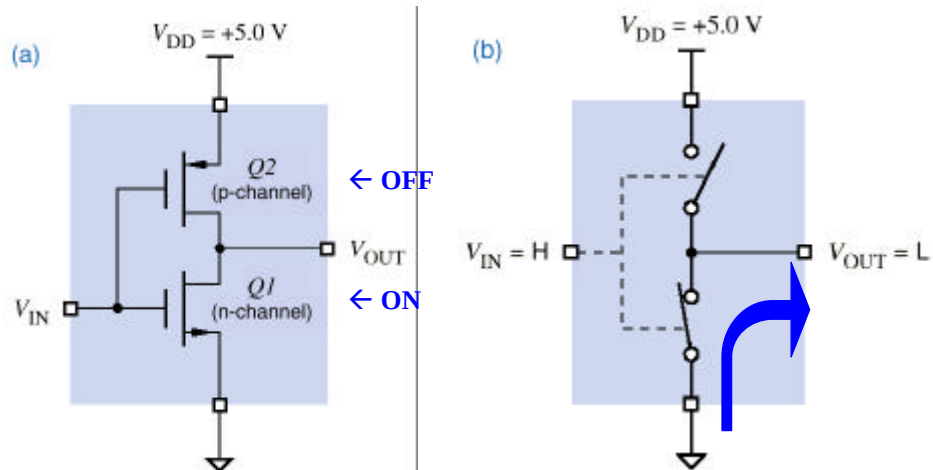


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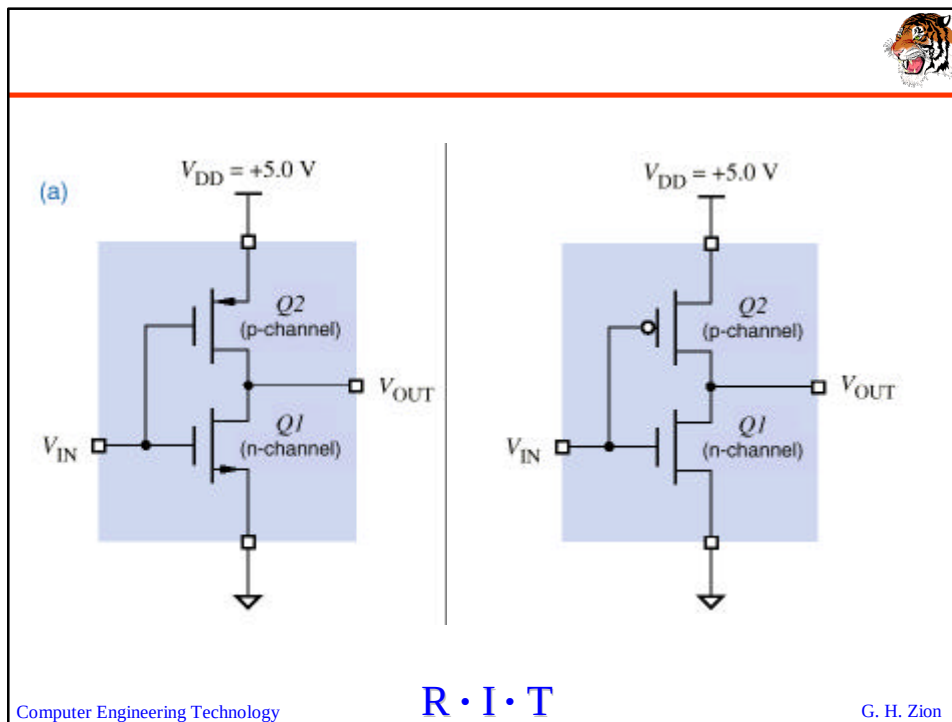
CMOS Inverter : High Input



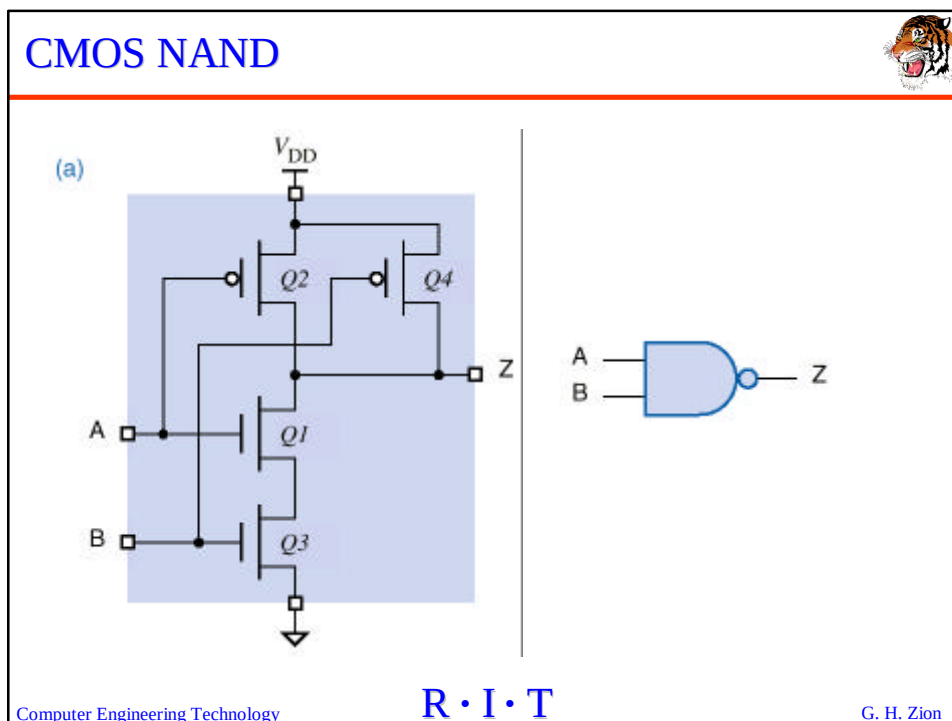
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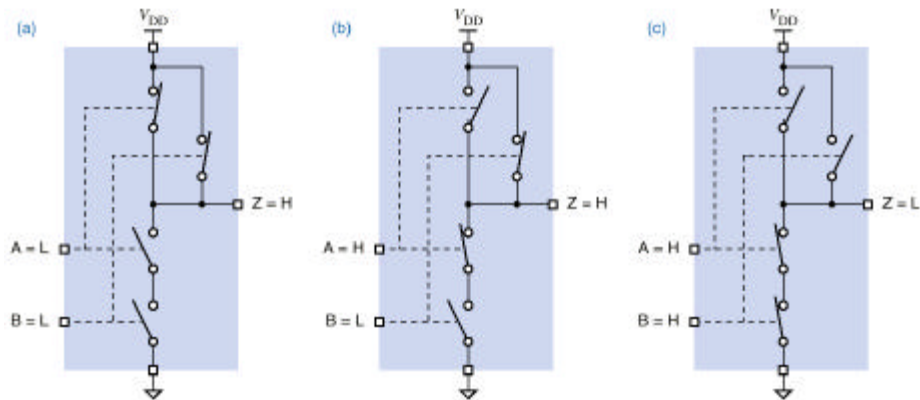
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CMOS NAND



CMOS NAND : Input Combinations

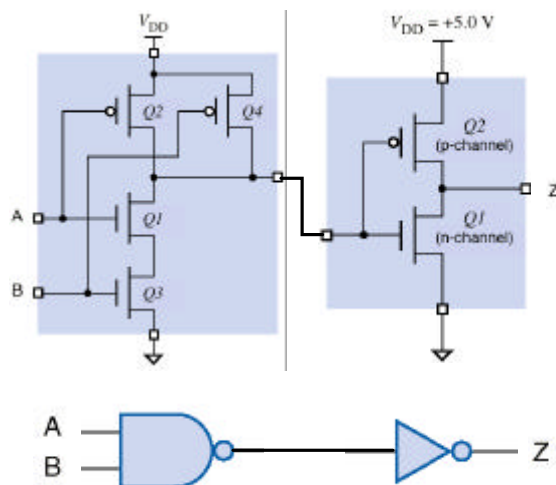


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Making An AND Gate

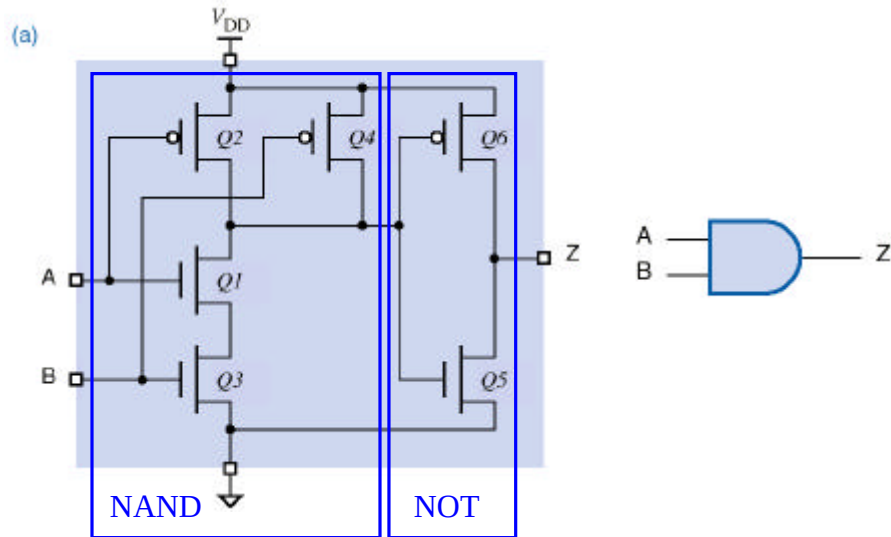


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CMOS AND

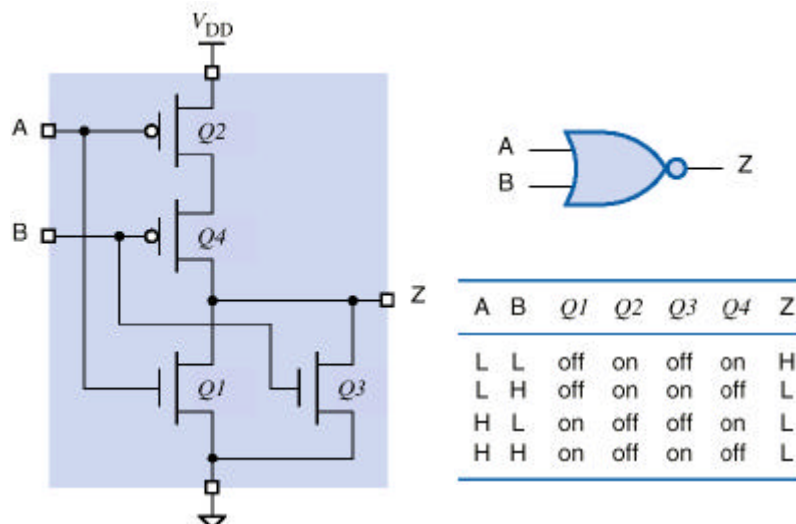


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CMOS NOR

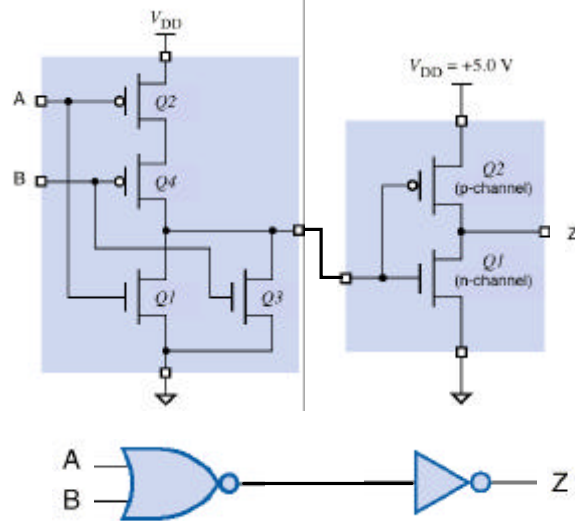


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Making An OR Gate

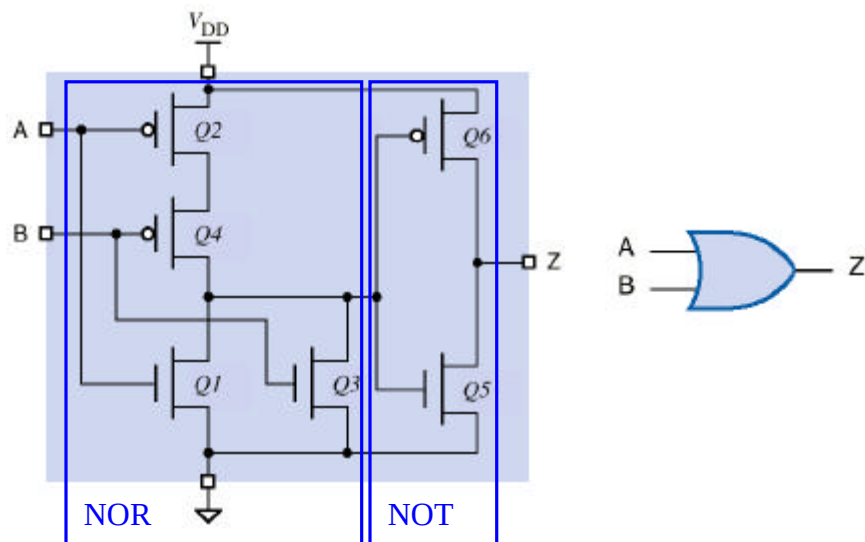


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CMOS OR



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CMOS Electrical Behavior



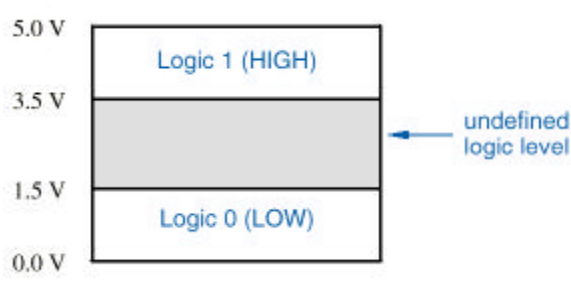
- Logic Voltage Levels
- DC Noise Margins
- Fanout
- Unused Inputs
- Current Spikes
- Transition Time
- Propagation Delay
- Power Consumption
- Schmitt-Trigger Inputs
- Tri-State Outputs
- Open-Drain Outputs

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Logic Levels – CMOS (generic)

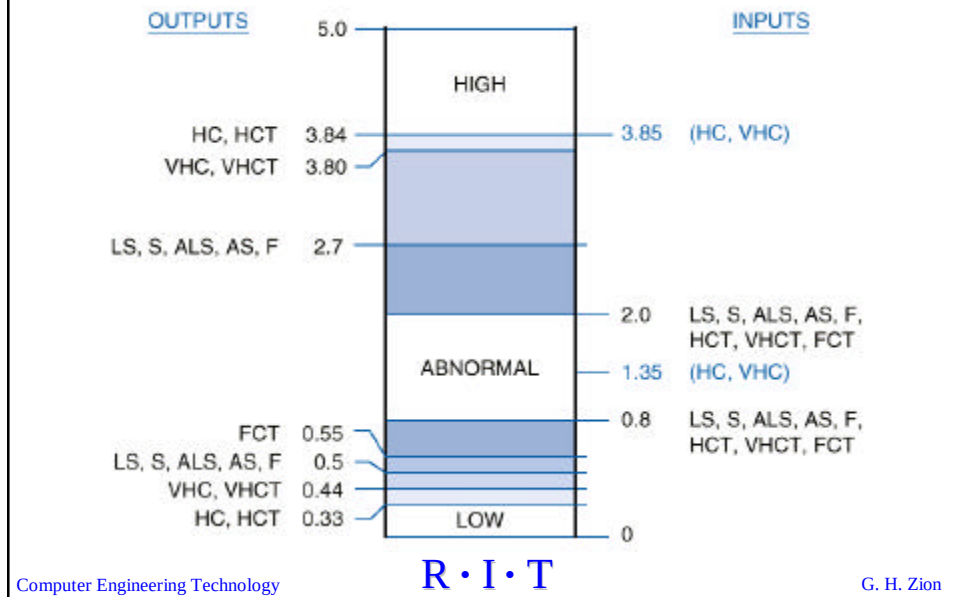


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Logic Levels – CMOS & TTL (specific)



DC Noise Margins

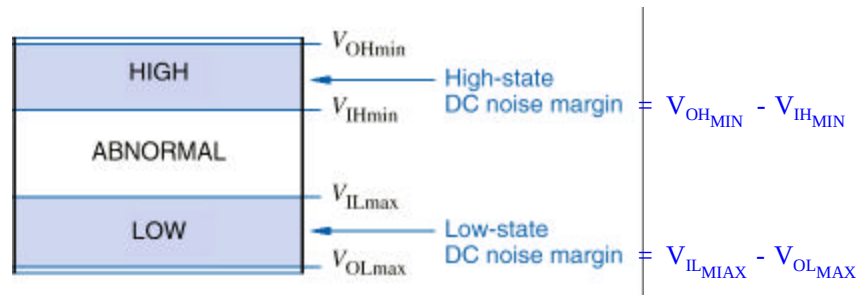


$V_{OH_{MIN}}$: The minimum output voltage in the HIGH state.

$V_{IH_{MIN}}$: The minimum input voltage guaranteed to be recognized as a HIGH.

$V_{OL_{MAX}}$: The maximum output voltage in the LOW state.

$V_{IL_{MAX}}$: The maximum input voltage guaranteed to be recognized as a LOW.

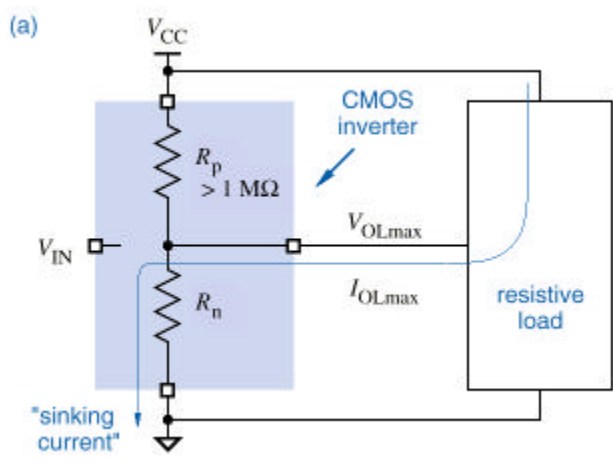


Fanout

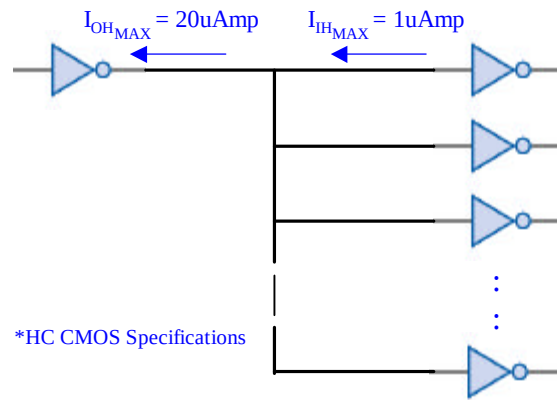


- The *fanout* of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications.
- *Fanout* must be examined for both possible output states.
- I_{OLMAX} : The maximum current that the output can sink in the LOW state while still maintaining an output voltage no greater than V_{OLMAX} .
- I_{OHMAX} : The maximum current that the output can source in the HIGH state while still maintaining an output voltage no less than V_{OHMIN} .

I_{OLMAX}

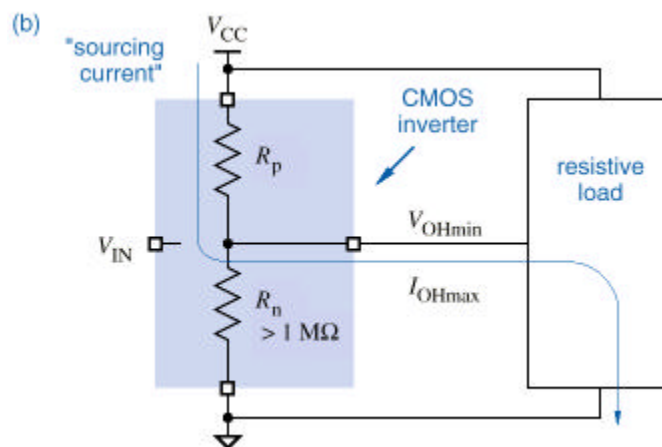


Fanout Example : Low Output

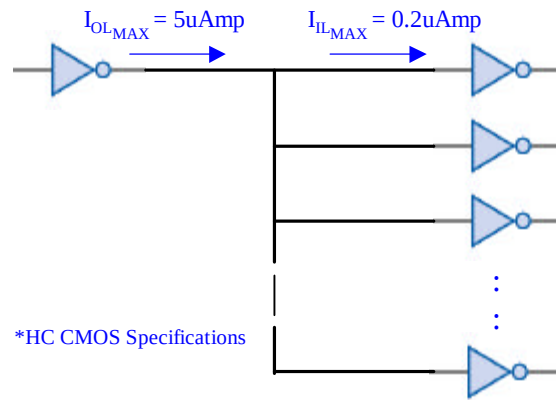


$$\text{Fanout}_{\text{LOW}} = \frac{I_{OH_{MAX}}}{I_{IH_{MAX}}} = 20$$

$I_{OH_{MAX}}$



Fanout Example : High Output



$$\text{Fanout}_{\text{HIGH}} = \frac{I_{OL_MAX}}{I_{IL_MAX}} = 25$$

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Exceeding Fanout - Loading



- In the LOW state, the output voltage (V_{OL}) will increase beyond V_{OL_MAX} .
- In the HIGH state, the output voltage (V_{OH}) will fall below V_{OH_MIN} .
- Propagation delay may increase beyond specifications.
- Switching times (rise times & fall times) may increase beyond specifications.
- The operating temperature will increase and may reduce the reliability and life of the part.

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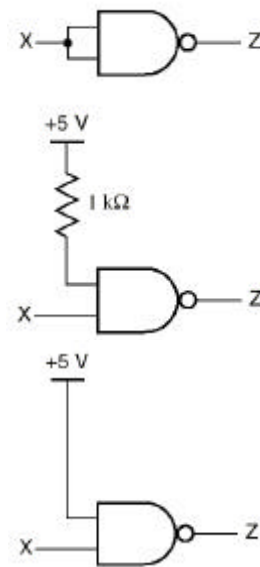
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Unused Inputs



- Unused inputs should never be left unconnected.
- All unused inputs should be pulled to a constant logic value.
 - HIGH for AND & NAND
 - LOW for OR & NOR
- Unused inputs can also be tied to another input.
 - Not preferred method for high-speed designs.
 - Additional input increases the capacitive load on the driving signal and thus reduces switching times (i.e. speed).



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Current Spikes and Decoupling Capacitors



- When a CMOS device switches from 0 to 5 volts, current flows from V_{cc} to GND through the partially-on PMOS and NMOS transistor.
- These currents, because they only occur briefly, cause current spikes and will show up as noise on the V_{cc} and GND connections.
- These current spikes need to be dampened with the use of decoupling capacitors between V_{cc} and GND.
- These decoupling capacitors need to be distributed throughout the circuit, typically one adjacent to each chip.

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Transition Time



- The time that the output logic take to change from one state to another is called *transition time*.
- Transition time has two components...
 - Rise time (t_r)
 - Fall time (t_f)
- The rise and fall times of CMOS outputs depend on the resistance of the “on” transistor and the load capacitance.
- The load capacitance comes from...
 - Input capacitance of load device (C_{THEVENIN})
 - Wire connecting the output to its inputs
 - Board capacitance.

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Transition Time : Rise Time / Fall Time



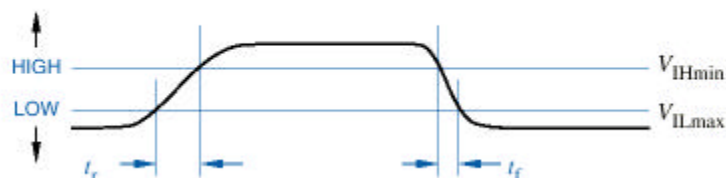
Ideal



Realistic



Actual



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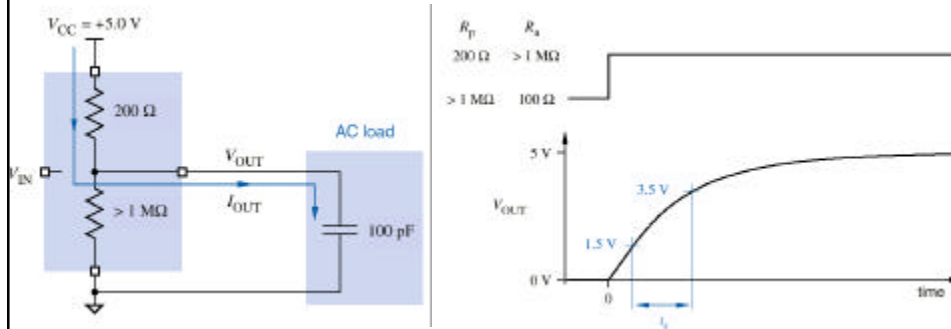
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Rise Time



Low-To-High Transition



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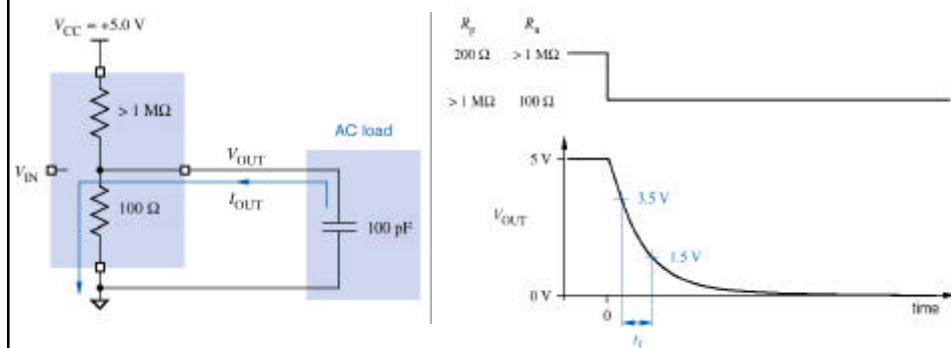
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Fall Time



High-To-Low Transition



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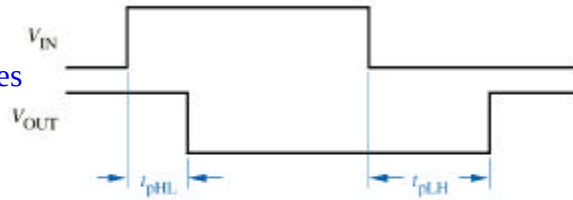
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Propagation Delay



The propagation delay of a signal path is the amount of time that it takes for a change in an input signal to produce a change in the output signal.

Ignoring Rise/Fall Times



Measured at Midpoints



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Power Consumption



- CMOS gates have to power consumption factors...
 - Static or quiescent power dissipation
 - Dynamic power dissipation
- Most CMOS devices have very little static power dissipation. This is one of the primary features of CMOS.
- CMOS device consume significant power only during transitions; this is called dynamic power dissipation.
- The dynamic power dissipation have two primary factors...
 - P_T : power dissipation due to output transitions.
 - P_C : power dissipation due to capacitive load.

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P_T : Output Transitions



$$P_T = C_{PD} V_{CC}^2 f$$

- P_T :
- C_{PD}
- V_{CC}^2
- f

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P_C : Capacitive Load



$$P_L = C_L V_{CC}^2 f$$

- P_L :
- C_{PD}
- V_{CC}^2
- f

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Schmitt-Trigger Inputs



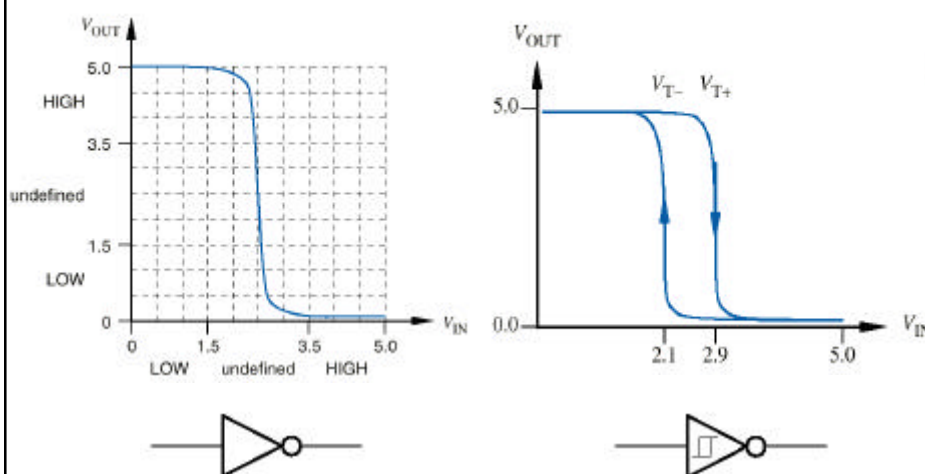
- A schmitt-trigger input uses feedback to shift the switching threshold voltage depending on whether the input is making a LOW-to-HIGH or HIGH-to-LOW transition.
- When the input is making a LOW-to-HIGH transition, the output will not change until the input has reached $V_{\text{THRESHOLD}+}$.
- When the input is making a HIGH-to-LOW transition, the output will not change until the input has reached $V_{\text{THRESHOLD}-}$.
- The difference between the two threshold voltages is called hysteresis. Schmitt-trigger inverters typically have a 0.8 V hysteresis.

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Transfer Characteristics



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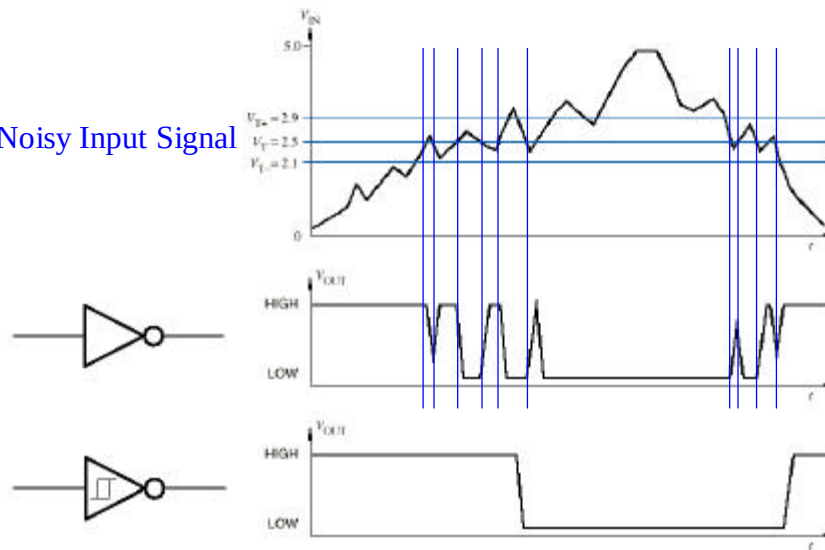
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Without Hysteresis



Noisy Input Signal



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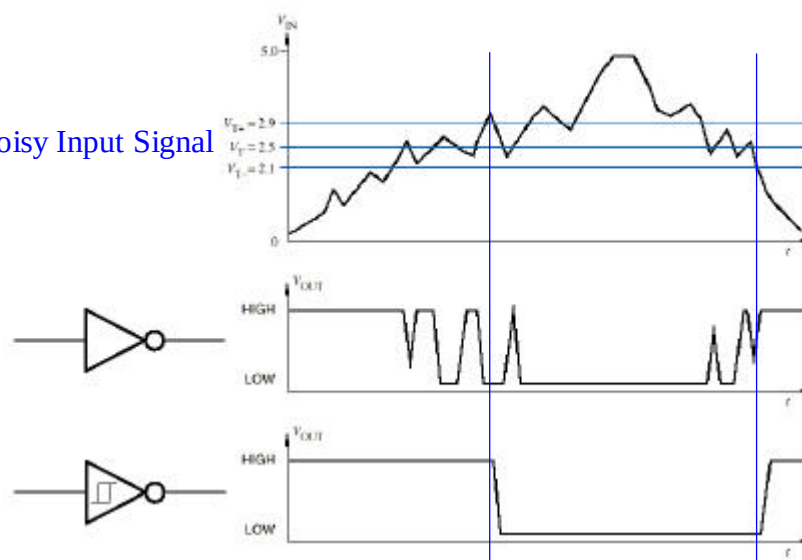
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With Hysteresis



Noisy Input Signal



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Tri-State Outputs



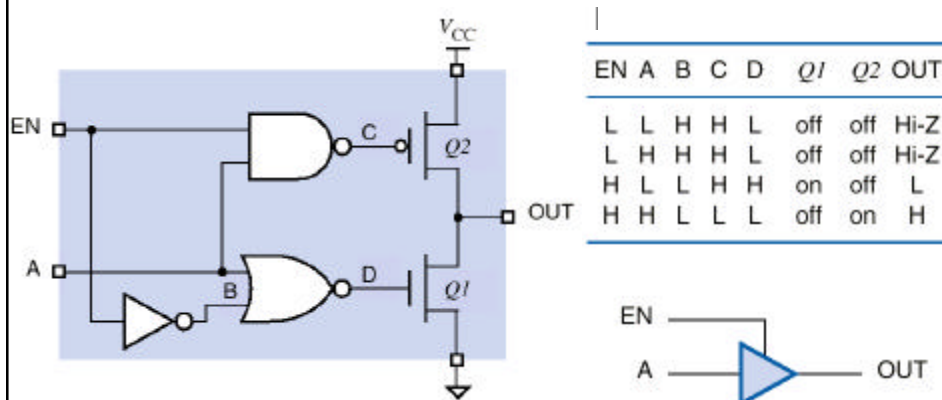
- The third logic state which is not a state at all. When an output is tri-stated it looks like a high impedance to any other device. Often called floating, or Z state.
- Requires an additional control input, typically called an enable. The enable controls whether the output is a LOW or HIGH (enabled) or Tri-States (disabled).
- Tri-state outputs are typically used where multiple outputs share a signal or bus. For example; data outputs on memory devices are tri-state outputs. Control circuitry is used to ensure that only one device is enabled at any given time (decode logic).

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Tri-State Buffer



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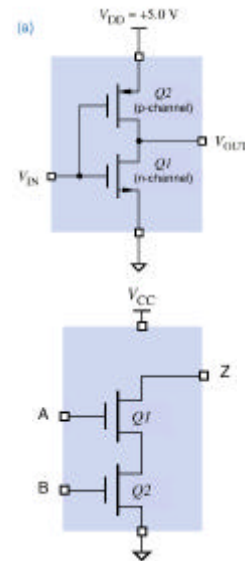
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Open-Drain Outputs



- In a CMOS device, the PMOS transistor provides for an active pull-up to V_{CC} .
- In an Open-Drain output, the drain of the top most NMOS transistor is connected to the output.
- Open-Drain outputs are used primarily for...
 - Driving LEDs
 - Driving Multi-Source Buses
 - Performing Wired Logic (to be discussed later)
- Different from Tri-State. Tri-State is H/L/Z, Open-Drain is L/Z only.

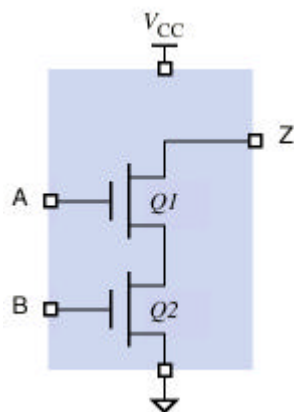


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Open Drain NAND



A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

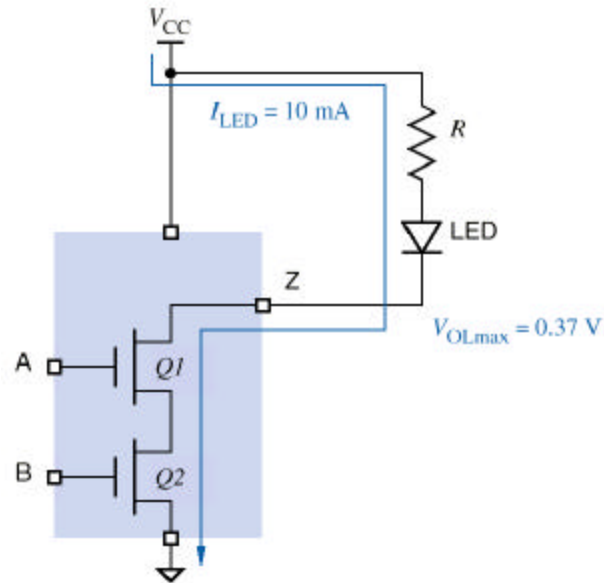


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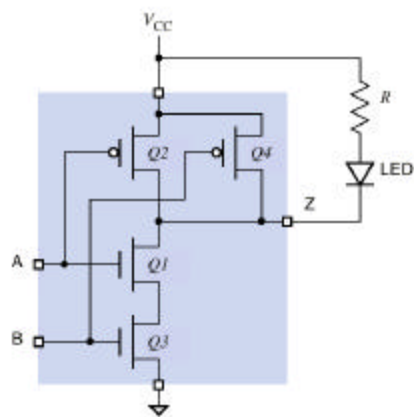
Driving LEDs



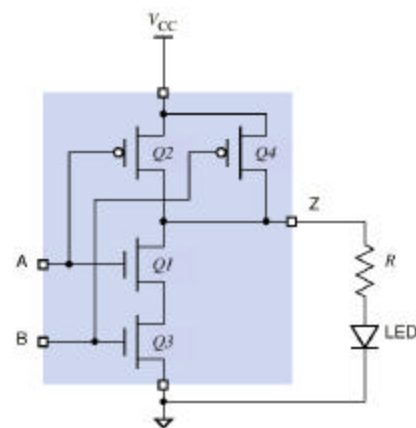
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Standard CMOS Can Drive A LED, But...



Sinking Current
LED is ON in the LOW state



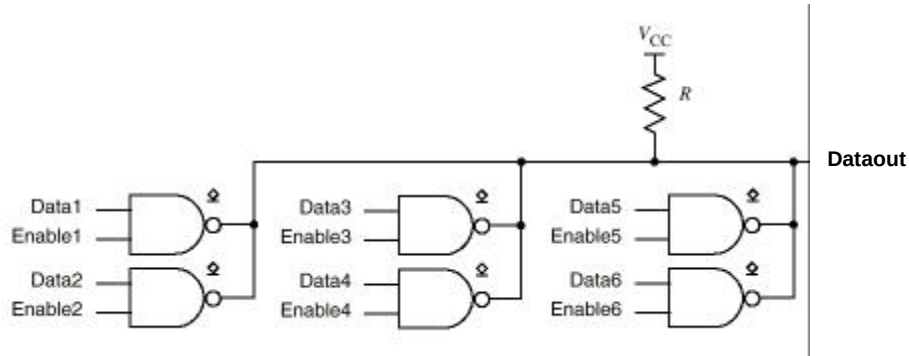
Sourcing Current
LED is ON in the HIGH state

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Driving Multi-Source Buses



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CMOS Logic Families



- First commercially available CMOS family was the 4000 series. Although the 4000-series offered low power consumption, they were slow and difficult to interface with the more popular (at the time) bipolar TTL family.
- 7400-series part naming : 74-FAM-nn...

The '74' prefix comes from the original numbering system created by Texas Instruments. Other company's use other numbering systems, but the 7400-series naming has become a pseudo-standard. (5400-series are the same part, but with military specifications).

'FAM' is an alphabetic family mnemonic. Only HC, HCT, VHC, VHCT, AHC and AHCT will be discussed.

'nn' signifies the function of the gate.

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HC and HCT Facts



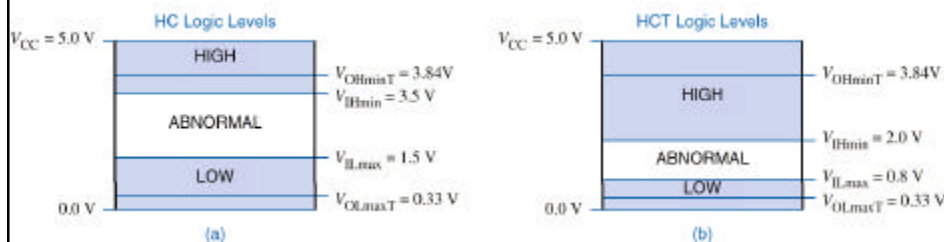
- HC = High-Speed CMOS
- HCT = High-Speed CMOS, TTL Compatible
- HC & HCT have high speed and better current sink/source capability than the 4000 family.
- The HC family was designed for use in CMOS only systems. Can operate with V_{CC} from 2 to 6 volts.
- The HCT family was designed to be used with TTL devices. V_{CC} is limited to 5 volts.
- Even when $V_{CC} = 5V$, HC devices are not quite compatible with TTL devices because of HC were designed to recognize CMOS input levels.

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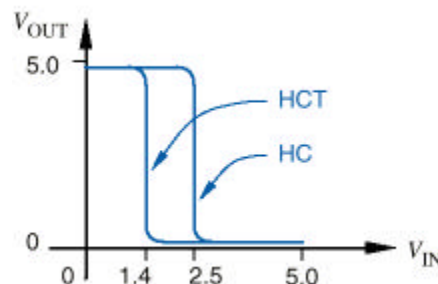
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HC & HCT Transfer Characteristics



These input level differences are set in the fabrication process by make transistors with different switching threshold voltages.



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VHC and VHCT



- VHC = Very High-Speed CMOS
- VHCT = Very High-Speed CMOS, TTL Compatible
- These families are about twice as fast as HC/HCT.
- Are backward compatible with predecessors (HC/HCT).
- VHC and VHCT differ from each other only in the input voltages that they recognize; their output characteristics are the same (like HC/HCT).
- HC/HCT and VHC/VHCT outputs have symmetrical output drive capability. They can sink and source equal amounts of current. Other families (ie FCT, TTL) have asymmetrical output drive capability.

Speed and Power Characteristics of CMOS



Table 3-5; Page 138

FCT and FCT-T



- FCT = Fast CMOS, TTL Compatible
- Able to meet or exceed the speed and drive capability of standard TTL while reducing power consumption and maintaining full TTL compatibility.
- The original FCT family produced a full 5V CMOS V_{OH} . This created enormous CV^2f power dissipation and circuit noise as the output switch from 0V to 5V in high speed applications (+25 MHz)
- FCT-T = Fast CMOS, TTL Compatible w/ TTL V_{OH} .
- The FCT-T maintained the high operating speed of the FCT while reducing both power consumption and switching noise.

Specifications for the 74FCT138T Device



Table 3-8; page 144